Design for Variability in DSM Technologies

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Abstract

Process-induced parameter variations cause performance fluctuations and are an important consideration in the design of high performance digital ICs. Until recently, it was sufficient to model die-to-die shifts in device (active) and wire (passive) parameters, leading to a natural worst-case design methodology [1, 2]. In the deep-submicron era, however, within-die variations in these same device and wire parameters become just as important. In fact, current integrated circuits are large enough that variations within the die are as large as variations from die-to-die. Furthermore, while die-to-die shifts are substantially independent of the design, within-die variations are profoundly influenced by the detailed physical implementation of the IC. This changes the fundamental view of process variability from something that is *imposed* on the design by the fabrication process to something that is *co-generated* between the design and the process.

This paper starts by examining the sources and historical trends in device and wire variability, distinguishing between inter-die and intra-die variations, and proposes techniques for design for variability (DOV) in the presence of both types of variations.

1 Sources of Variability

From a designer's point of view, IC performance variability is impacted by two distinct sets of factors:

- *Environmental factors* which include variations in power supply voltage, noise coupling among nets and temperature. These factors have time constants determined by the operation of the IC and are typically in the range $10^{-9} \cdots 10^{-3} s$ range and have always been analyzed at the intra-die level.
- *Physical factors* are caused by processing and mask imperfections and reliability-related degradation. They have time constants that are determined by the fabrication and wear cycles and are typically in the range $10^{6} \cdots 10^{9} s$. These factors were traditionally modeled as intra-die shifts in electrical parameters, but their within-die component is rapidly becoming just as important.

Although both sources of variations are important for a manufacturable design, this paper will deal only with the physical sources of variability, which we denote by $\mathcal{P}$, and which include all device and wire model parameters such as V_{th}, T_{ox} and R_S.

If $\mathcal{P}$ is *constant* within a die, but varies within a wafer or lot, then $\mathcal{P}$ is independent of local differences within the chip, and we can treat variations in $\mathcal{P}$ as variability *imposed* upon the circuit. Such variability can be analyzed using classical worst-case or Monte-Carlo techniques [1], and all that is required is the probability distribution describing $\mathcal{P}$.

When $\mathcal{P}$ varies within a die because (a) the die is large relative to the wafer, or (b) $\mathcal{P}$ has a strong layout dependence (e.g. the polysilicon nested vs. isolated effect [3]). Determining the design performance variation becomes harder because the number of entities varying is larger but there are analysis techniques to estimates the resulting variation, see for example [4, 5].

2 Trends in Variability

While one can infer quite a bit from studies of trends in device and wire parameters such as the 1997 SIA technology roadmap[6], it is important to relate those studies back to some technology-independent metric in order to evaluate overall trends in variability. To this end, consider the circuit in figure 1 composed of a source buffer driving an identical destination buffer through a length of minimum-width wire. We strive to examine the trend in the relative impact of wire and device variability on the delay for various technology generations. Across technologies we choose to maintain the W/L ratio for the buffer and find the maximum wire length beyond which inserting another buffer between the source and destination would lower

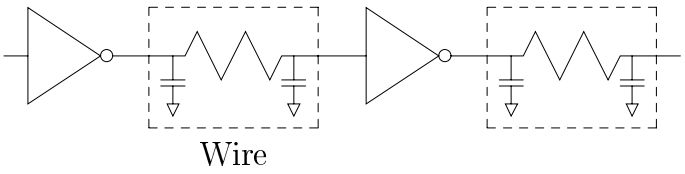

Figure 1: Canonical circuit.

	1997	1999	2002	2005	2006
L_{eff} (nm)	250	180	130	100	70
T_{ox} (nm)	5	4.5	4	3.5	3
V_{dd} (V)	2.5	1.8	1.5	1.2	0.9
V_T (V)	0.5	0.45	0.4	0.35	0.3
W (μ)	0.8	0.65	0.5	0.4	0.3
H (μ)	1.2	1.0	0.9	0.8	0.7
ρ ($\frac{m\Omega}{\Box}$)	45	50	55	60	75
L_{max} (μ)	*2123*	*1920*	*1670*	*1526*	*1303*

Table I: Technology parameters.

overall delay. This maximum wire length is estimated following [7] as $L_{max} = \sqrt{2(\tau_B + R_B C_B)/R_w C_w}$, where τ_B, R_B and C_B are the delay, output resistance and input capacitance of the buffer, and R_w and C_w are per unit length of the wire.

We chose five technologies in the 250 to 70 nm gate length range conforming to the 1997 SIA technology roadmap, and computed L_{max}. The results are shown in table I and figure 2 which explains the wire geometrical parameters. The salient feature is a super-linear (relative to L_{eff}) decrease in L_{max} vs. process generation, which shows the well publicized increase in the influence of interconnect.

We then considered the impact of device and wire variations on the delay of this buffer/wire combination assuming tolerances conforming broadly to SIA roadmap numbers (see Table II) with some exceptions based on early experience with IBM technologies. Figure 3 shows the tolerances expressed as percentages, which more clearly shows the current trends in the various components. The contributions of of device and wire variability to total delay variability remain fairly constant (table III) which is important because it means that this simple circuit is a good canonical gauge to differentiate circuits based on their sensitivity to device and wire variations. If we perform similar simulations without scaling transistor widths (table III, A), or scaling wire length at the same rate as L_{eff}, (table III, B), we get very different results.

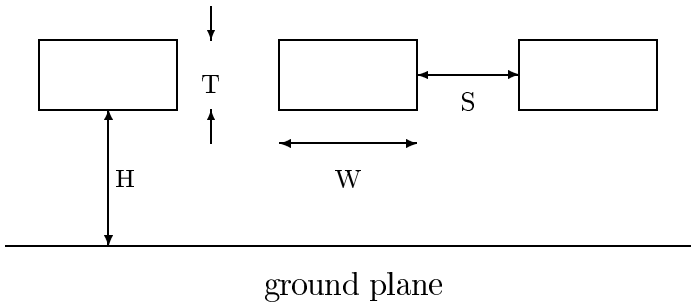

Figure 2: Cross-section showing wire geometry.

2.1 Within-Die Variation Trends

The impact of within-die variability of device parameters has been well studied [5] but wire variability has only recently been studied [8]. This is difficult because within-die variation is composed of *systematic* (layout dependent) and *random* components, and the analysis of the systematic component cannot occur until the layout is substantially complete. Early in the design cycle, all within-die variation is random, as the design is completed, part of the variations becomes assesable from models for the systematic component.

Figure 3 showed the general trend in total variation. Over the same time span, we see the proportion of L_{eff} variations that is within-die go from 40% to 65%. To determine the relative impact of the increase in the various components of within-die variations we performed simulations and modeled the delay of the circuit in terms of the basic technology variables:

$$Delay = D_0(1 + C_{L_{eff}} L_{eff} + C_{V_T} V_T + ...) \qquad (1)$$

We then scaled the model coefficients by the expected within-die variability in each of the variables. The results are expressed as percentages in table IV and they show -interestingly- that wire resistivity is becoming one of the dominant source of delay variability. This points to the need for more aggressive use of buffer insertion [7] and wire sizing to control delay variability.

3 Analysis with Variability

The goal of parameter variability analysis is to predict their impact on circuit performance variability hence design tolerances and ultimately yield. This subject has a rich academic research heritage[9, 10] which -unfortunately- has not always successfully permeated

through EDA tools to reach circuit designers. The exceptions in this area are worst-case analysis [11, 12, 2], which is usually supported directly by manufacturing process characterization organizations, and Monte-Carlo analysis, which is part of most modern circuit simulators such as Spice [13].

Observing the trends above, one can identify three sets of issues for analysis of variability in the DSM regime. We deal with these issues in the following: subsections.

3.1 Inter-Die vs. Intra-Die Variations

Substantially all of existing practical and theoretical work on yield analysis and maximization techniques has focused on intra-die variations. Where within-die variations were taken into account, primarily in analog design, the variations were characterized as mismatch between specified devices. If the number of such mismatches is small, the same worst-case techniques applied to inter-die variations can be used.

The issue is somewhat more complicated when *all* potential mismatches are to be taken into account, but the problem can be cast in a form that remains tractable [4].

3.2 Deterministic Variations: Variability vs. Uncertainty

Since a substantial portion of within-die variability is design (layout) dependent [14, 8], and therefore deterministic, one can assume that its impact can be assessed and *tuned* out of the design. This is often not possible, however, because:

- Models for the design dependence of a particular parameter may not exist, may not be sufficiently accurate, or may simply be too expensive to evaluate.
- Early in the design cycle, the design is only defined at higher levels of abstraction and therefore the detailed interaction with the physical implementation can only be estimated.
- A design which is meant to be reusable (i.e. an IP block) cannot pre-determine the physical design environment in which it will operate.

In such cases, the deterministic variability of a parameter exhibits itself as *uncertainty* in the parameter value and effectively randomizes that parameter.

	1997	1999	2002	2005	2006
L_{eff} (nm)	80	60	45	40	33
T_{ox} (nm)	0.4	0.36	0.39	0.42	0.48
V_{dd} (V)	0.25	0.18	0.15	0.12	0.09
V_T (V)	50	45	40	40	40
W (μ)	0.2	0.17	0.14	0.12	0.1
H (μ)	0.3	0.3	0.27	0.27	0.25
ρ ($\frac{m\Omega}{\Box}$)	10	12	15	19	25

Table II: Technology parameter 3σ variations.

3.3 Simulation Cost

Detailed study of the impact of process variability on design performance has traditionally been done using circuit simulators such Spice. This was accomplished by analyzing necessarily small but relevant parts of the design one at a time.

In order to do full-chip analysis of variability, the analysis techniques *must* be capable of being applied at the static timing level, since this is the only simulation methodology capable of dealing with a complete modern design. This introduces a number of difficulties, primarily due to the perception that the error margin in performance estimates derived from static analysis is large. Nevertheless, relevant examples are starting to become available [8, 15].

4 Conclusions

As we march headlong into the sub-tenth micron era, the following observations about variability can be made.

- Variability as a whole is increasing and the within-die portion of the whole is also increasing.
- Wire variability, especially in wire resistance, is not negligible and needs to be analyzed to the same degree as active device variability.
- Current process characterization methodologies focus on inter-die worst-case variations and need to expand to provide deterministic and statistical models of intra-die variations.
- The current generation of CAD simulation and analysis tools can only deal with worst-case analysis and Monte-Carlo analysis. We -the practitioners- need to ensure that design-for-variability techniques are developed and integrated into existing and future design environments.

	1997	1999	2002	2005	2006
Constant W/L, wire length = L_{max}					
Device (%)	47	47	44	44	45
Wire (%)	53	53	56	56	54
Case (A): no scaling of device width					
Device (%)	47	43	37	35	34
Wire (%)	53	57	63	65	66
Case (B): scale wire length with L_{eff}					
Device (%)	47	51	52	55	60
Wire (%)	53	49	48	45	40

Table III: Device and wire contribution to delay variations.

	1997	1999	2002	2005	2006
V_{dd}	9.5	10.8	10.0	9.5	8.9
Device					
T_{ox}	1.3	2.5	3.2	3.9	4.9
V_T	3.8	5.3	5.5	6.5	7.2
L_{eff}	32.4	28.3	25.5	24.6	23.8
Wire					
W	13.3	12.0	11.7	11.4	10.5
S	9.3	9.4	9.9	9.5	9.4
T	6.8	7.0	8.0	8.2	8.2
H	7.8	8.0	8.1	8.3	7.1
ρ	16.0	16.6	17.9	18.4	20.1

Table IV: Impact of within-die variation on delay.

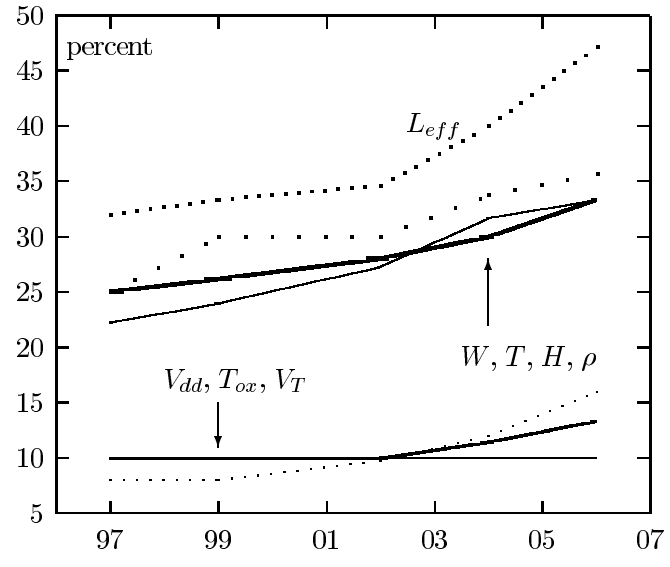

Figure 3: Technology parameter variations.

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