A Performance Comparison between Hardened-by-Design and Conventional-Design Standard Cells

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Abstract— **Several Radiation-Hardened-By-Design (RHBD) standard cells have been designed using ground rules for a commercial TSMC 0.3 μm CMOS technology. Post-layout simulations have been performed at the transistor level. The occupied silicon area, together with the timing and power performance of the RHBD standard cells, are compared with regular minimum-area layouts designed with the same process. The performance comparison is also made with respect to commercial standard cells designed with two older CMOS processes (TSMC 0.4 μm, HP 0.6 μm). These older technologies were chosen to represent the performance of some of the rad-hard processes that are still in production.**

***Index Terms*—Radiation Hardness, RHBD, Standard Cells, Total-dose Tolerance, Enclosed Layout Transistors (ELT), Edgeless Transistors**

I. Introduction

OVER the years, various methods have been used to make integrated circuits tolerant to radiation for application in aerospace systems, military environment electronics, and measurement equipment in high-energy physics (HEP) experiments. The radiation hardness is a key issue for these critical systems since they need to function accurately and consistently in their intended environment of use, which may subject them to radiation. The required radiation tolerance has been traditionally achieved using particular manufacturing processes specifically created to obtain radiation-hardness. However, the development of these processes was typically supported by defense funds and many semiconductor manufacturers abandoned the rad-hard process market after the end of the cold war. Today, few radiation-hardened processes are available and the semiconductor market is largely driven by commercial applications. The complexity overhead of specialized rad-hard technology, coupled with the low-volume demand, produced an unavoidable performance gap with respect to the state-of-the-art commercial processes. As a result, radiation-hardened technologies are usually at least two generations behind the commercial ones. Moreover, the fast reduction of the gate oxide thickness due to the fabrication technology improvement makes the active devices used in commercial deep sub-micron CMOS processes inherently more tolerant to total-dose radiation effects [1]-[3]. Consequently, they are more attractive for space applications. In particular, threshold voltage shifts induced by total ionizing dose becomes less significant as the gate oxide thickness decreases. As a result, leakage currents associated with transistor edge effects and due to field-oxide trapped charges are the most important total-dose effects in modern CMOS integrated circuits.

These issues, together with the wide availability of commercial CMOS processes led to the development of Radiation-Hardness-By-Design (RHBD) techniques [4]-[6]. The RHBD approach consists of employing specified layout and circuit design techniques to create radiation-tolerant ICs with low-cost, widely available, commercial CMOS technologies. As an example, edgeless NMOS transistors, also called Enclosed Layout Transistors (ELTs), are used to eliminate radiation-induced edge leakage currents. At the same time, guard banding around the devices reduces the field oxide leakage and the susceptibility of the circuits to the latch-up phenomenon [4], [5]. On the other hand, Single Event Upset (SEU) problems in digital circuits can be addressed at a higher design level by latch redundancy methods [7], or by employing SEU-hardened latch designs like in [8].

The drawbacks of the RHBD solutions are basically the high W/L ratio required by the use of edgeless transistors and

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the area penalty necessary to implement both the layout and the latch redundancy techniques. In other words, the RHBD approach trades circuit density for radiation hardness.

In this work, some of the gate-level layout hardness-by-design techniques are applied to create a RHBD standard-cell library using a 0.3 µm commercial CMOS process. The layout design choices resulting from trade-offs among silicon area, radiation tolerance, and cell performance are described. In addition, the area requirements and simulated performance of the RHBD standard cells are compared to circuits realized in the same commercial technology with minimum area layouts. The same comparisons are also made with respect to minimum area standard cells designed using older 0.4 µm and 0.6 µm CMOS processes that may represent the performance and area requirements of circuits designed for rad-hard processes without using special layout techniques.

The simulation results reveal similar performance for the RHBD cells and the minimum-area ones designed in the previous technology generation. However, the RHBD library performs much better than designs from a technology that is two generations older, which is typical of the amount by which radiation-hardened processes trail mainstream commercial processes.

II. Standard Cells Design

Several combinatorial RHBD standard cells were designed using the commercial TSMC 0.3 µm, 5-metal, 1-poly, CMOS technology design rules. When designing RHBD full-custom layouts, trade-offs must be made between the application of radiation-hardening techniques and the relevant area penalty, while minimizing the parasitic capacitance of the source/drain diffusions in order to preserve the cell's dynamic performance. Techniques used include edgeless transistors, guard rings, and power/ground bus widening.

First, edgeless NMOS and PMOS transistors are employed in the RHBD standard cells. These re-entrant transistors, characterized by a ring-shaped gate, eliminate the presence of the thin-to-thick oxide edge between source and drain, thus completely eliminating the edge leakage currents.

Guard rings around both NMOS and PMOS devices are always used in the cells designed as part of this work. They consist of N-plus diffusions surrounding the PMOS devices in the N-well region, and of P-plus diffusions surrounding the NMOS devices on the P-type substrate. Their main effect is limiting the field oxide leakage between the MOSFETs by actually interrupting the leakage path. They also significantly reduce the single event latch-up (SEL) probability. This is because the introduction of P-plus guardbands in the N-well region and N-plus guardbands in the P-type substrate reduces the gain of the parasitic bipolar transistors that are responsible for the latch-up phenomenon. It's worth noting that in most of the gates, two NMOS or two PMOS transistors can be placed inside a single guard ring, still avoiding the presence of field-oxide leakage paths.

Finally, ground and power metal busses are widened by about 60% with respect to regular designs in order to prevent supply voltage drops induced by high dose-rate events.

The minimum width value (W) for an edgeless NMOS transistor, according to the chosen technology layout rules, is fixed at 4.8 µm. This value determines the minimum area of the RHBD cells. The size of the PMOS transistors is always chosen to match the driving capability of the NMOS devices, obtaining approximately the same propagation delays both for rising and falling edges. The edgeless shape is therefore used also for the PMOS devices since this layout style provides an area-efficient way to obtain the required large W/L ratio.

The same standard-cell functions of the RHBD library were designed for minimum area, without RHBD techniques for comparison in the TSMC 0.3 µm process. The design of the minimum-area layout was also scaled for two older CMOS processes: TSMC 0.4 µm (4-metal, 1-poly) and HP 0.6 µm (3-metal, 1-poly). A comparison of the RHBD standard cells with these latter designs is interesting because they are similar to typical specialized rad-hard technologies in terms of performance and circuit density. For all the commercial designs, the NMOS width was set to the minimum width of a source/drain contact, while the PMOS width was again determined to obtain symmetric dynamic response.

III. Area Comparison

Fig. 1 shows layout views of the and-or-invert AOI22 gate designed in the four technologies described above. This particular four-input cell is composed of eight MOS transistors and realizes the logic function $Y = \overline{AB + CD}$. The

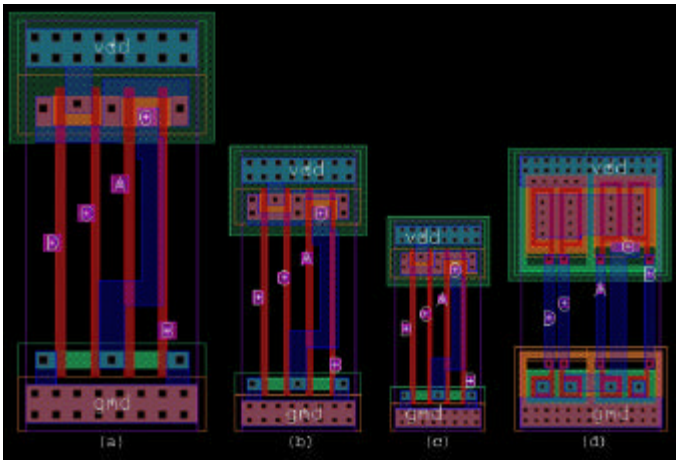

Fig. 1. Layout views for the AOI22 std. cell of 4 different libraries: commercial (a) HP 0.6 µm, (b) TSMC 0.4 µm, (c) TSMC 0.3 µm CMOS processes and (d) RHBD TSMC 0.3 µm.

height of the standard cells was chosen to be 20 µm for the RHBD library and 15 µm, 20 µm and 30 µm for the 0.3 µm, 0.4 µm and 0.6 µm commercial libraries, respectively.

Detailed results of the area comparison among the different libraries are presented in Fig. 2, in which the area ratio between the RHBD cell and the other technologies is reported for cell functions of increasing complexity. It can be

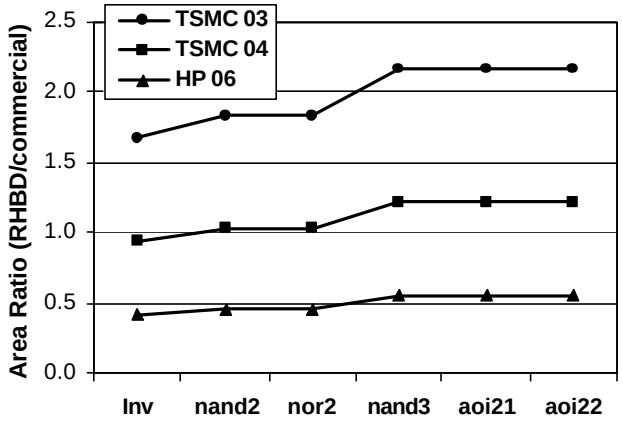

Fig. 2. Area ratio between RHBD and commercial standard cells designed in three different technologies (TSMC 0.3 µm, TSMC 0.4 µm, and HP 0.6 µm), for logic functions of increasing complexity (number of transistors).

noted that the RHBD cell areas are approximately twice those of the minimum-area cells in the same technology, but still about half those required for minimum-area designs in the 0.6 µm process. The RHBD cell areas are approximately the same as those of minimum-area cells designed in the 0.4 µm technology library.

A step increase of the area ratio can be observed from the NOR2 function to the NAND3 function. This is due to the need for two different guard-rings instead of one in the RHBD layout. It is also worth observing that the area ratio slightly increases with the cell complexity.

IV. Performance Comparison

The four sets of standard cells were extensively simulated using foundry-provided SPECTRE models in the CADENCE design environment. The value of the parasitic capacitances associated with source and drain area and perimeter were extracted from the layout and precisely taken into account. In each simulation, the cells were loaded with two inputs of equivalent gates fabricated in the same technology (FO = 2) and an additional capacitance representing the interconnections. The value of the latter capacitance was chosen to be 20 fF for the TSMC 0.3 µm technology and scaled for the other processes. Typical-mean process parameters were used to perform the simulations. The supply voltage was set to 2.5 V for the TSMC 0.3 µm process, 3.3 V for the TSMC 0.4 µm process, and 5 V for the HP 0.6 µm process.

For each cell and for each library, several performance parameters, such as propagation delay (t_{pd}), power dissipation, and maximum operating frequency, were obtained from the simulation results. In order to compare the RHBD and minimum-area versions of the standard cells realized with the TSMC 0.3 µm process, the values of some significant performance parameter ratios are reported in Fig. 3, for several types of logic functions. As for the area, the ratios are always calculated by dividing the RHBD parameter value by the corresponding minimum-area one. In the figure, PDP is

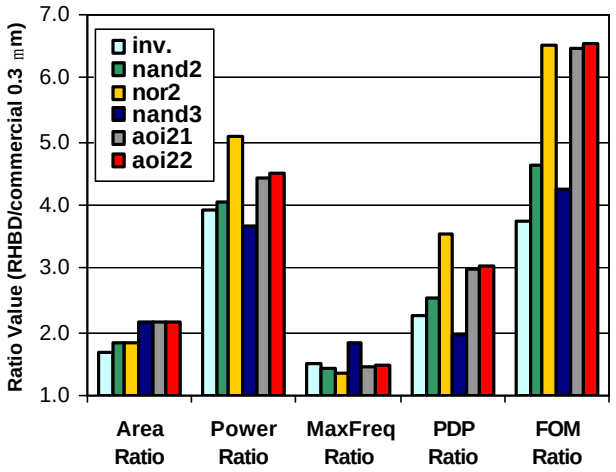

Fig. 3. Performance parameter ratios between minimum area RHBD standard cells and minimum area commercial design, both realized in the TSMC 0.3 µm CMOS technology.

the power-delay product and FOM stands for figure of merit (power × delay × area).

Figure 3 shows that passing from minimum-area commercial standard cells to RHBD cells with the same technology produces a power dissipation penalty of about a factor of four. On the other hand, the RHBD cells are about 1.5 times faster than the minimum-area ones due to the higher *W/L* ratio.

The differences in the ratio values between the cell types are due to the value and topological position of the parasitic capacitances relevant to the source and drain regions in the RHBD layout. From this point of view, the NOR gate has the worst behavior due to the presence of a series combination of

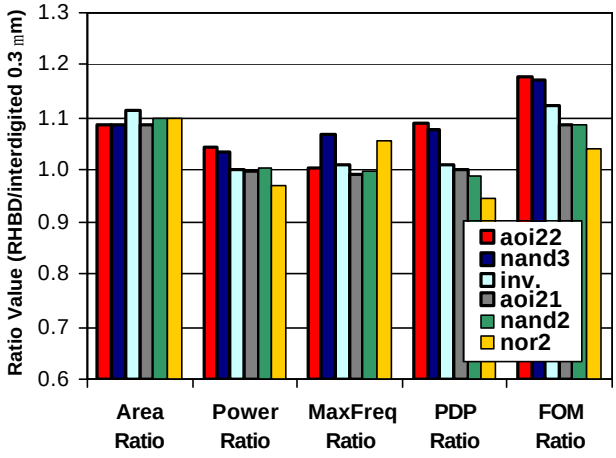

Fig. 4. Performance parameter ratios between RHBD standard cells and regular design with equal transistor width and inter-digitated transistors shape. Both designs are realized in the TSMC 0.3 µm CMOS technology.

two large PMOS transistors. In particular, with this circuit topology, the relatively high parasitic capacitance related to the area between the edgeless PMOS transistors and the relevant guard ring must be placed in the intermediate node of the series.

For further analysis of the effect of the RHBD-layout parasitic capacitances, regular cells were also designed with the same transistor width (*W*) as the RHBD cells, using inter-digitated layout shapes (but still in the TSMC 0.3 µm process). The comparison between the post-layout simulation results is reported in Fig. 4.

The ratios values show similar power dissipation and maximum operating frequency because the parasitic capacitance effects in the two approaches are similar. The

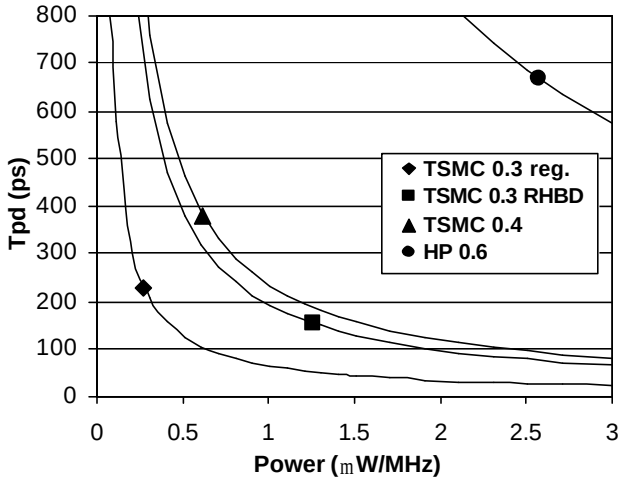

Fig. 5. Power delay diagram for the AOI22 gate, realized with RHBD 0.3 µm CMOS process and with three different commercial scaling technologies (TSMC 0.3 µm, TSMC 0.4 µm, and HP 0.6 µm). Equal power-delay-product curves are reported in the plot.

comparison also reveals that there is an area penalty for the RHBD cells of about 10%, resulting in a FOM ratio always greater than unity.

As an example of comparison between technologies, the power-delay performance of the AOI22 gate is reported in Fig. 5 for the four different technologies. Relevant equal PDP curves are also represented.

The figure shows that the RHBD cell is the fastest when compared to the three minimum-area designs because of the large *W/L* ratio required for the ELTs. Both the power consumption and the propagation delay for the HP 0.6 µm technology are clearly greater than the RHBD cell, indicating the benefits of the RHBD design. When compared in particular to the TSMC 0.4 µm design, the RHBD gate dissipates more power in exchange for faster transient response. The resulting power-delay product is similar for the two technologies.

Considering also the occupied silicon area in the comparison, the values of some significant performance parameter ratios are reported in Fig. 6, still particularly for the AOI22 gate. Since the occupied silicon area is also similar, the resulting FOM ratio is very near unity.

A more detailed comparison between the RHBD 0.3 µm and the minimum-area 0.4 µm libraries is shown in Fig. 7, where the performance parameter ratios between the two technologies are reported. The figure shows that the considerations for the AOI22 gate are true also for the other logic functions, with slight differences due to the different

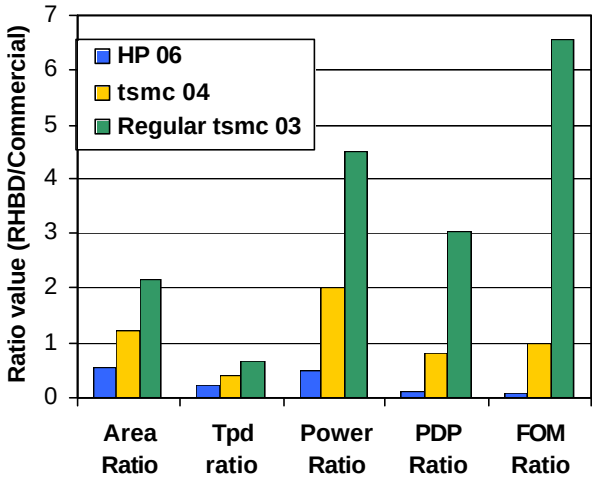

Fig. 6. Some significant performance parameters ratios between the TSMC 0.3 µm RHBD approach and commercial AOI22 std. cells realized in the 3 different scaling technologies.

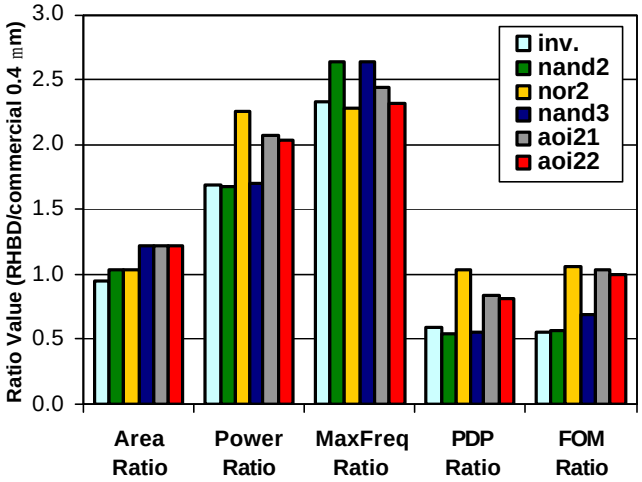

Fig. 7. Comparison between RHBD TSMC 0.3 µm standard cells and the same standard cells designed with the 0.4 µm CMOS technology, with minimum area design and without radiation hardening techniques.

effect of the parasitic capacitances. In particular, in the layouts of the inverter and the NAND gates, the large parasitic capacitance associated with the external terminal of the PMOS edgeless transistors can be shorted to V_{dd}, preserving the cell dynamic performance. For this reason the PDP ratio and consequently the FOM ratio are significantly below unity for these logic functions.

Finally, the single FOM ratio between the RHBD cells and the commercial technologies is represented in Fig. 8 for several logic functions in order to compare the overall performance of the different libraries. The FOM value of the 0.3 µm RHBD cells is always better than the HP 0.6 µm designs (at least by a factor of four), whereas the ratio corresponding to the TSMC 0.4 µm technology ranges from significantly below unity to unity, depending on the logic function.

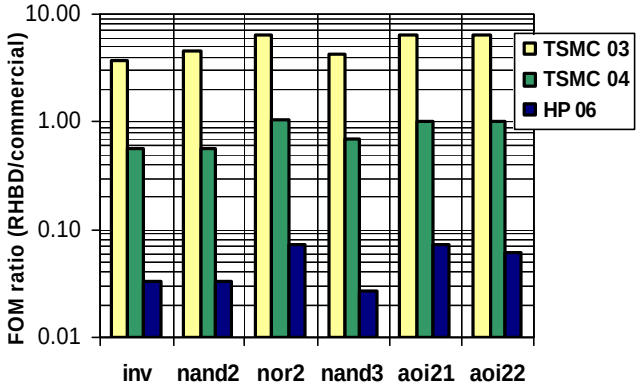

Fig. 8. FOM (Figure of Merit: Power × delay × area) ratio between RHBD and minimum-area designs for three different commercial processes (TSMC 0.3 µm, TSMC 0.4 µm, HP 0.6 µm) and for six different types of standard cells.

V. Conclusion

A Radiation-Hardened-By-Design standard-cell library was developed using ground rules for the TSMC 0.3 µm CMOS process. Its performance is compared to minimum-area standard-cell libraries realized in three different technologies (TSMC 0.3 µm, TSMC 0.4 µm, and HP 0.6 µm). Post-layout simulation results show that the performance metrics for the 0.3 µm RHBD cells for the chosen technology are similar to those obtained for minimum-area designs in the previous process generation (0.4 µm). The 0.3 µm RHBD standard cells have significant advantages in the areas of density, power consumption, and transient response compared to designs executed in a technology that is two generations older (typical of the amount by which typical radiation-hardened processes trail mainstream commercial processes).

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