

A Low Cost Inductorless Low Noise Amplifier for ISM Bands

Pedro Jesus^{1,2}, Miguel Andrade Martins¹, Jorge R. Fernandes^{1,2}

¹INESC-ID / ²Instituto Superior Técnico, TU Lisbon

Rua Alves Redol, 9; 1000-029 Lisboa

{pedro.jesus,miguel.martins,jorge.fernandes}@inesc-id.pt

Abstract— In this paper, we present a low-cost wideband inductorless low noise amplifier for applications operating in the ISM sub-GHz bands. The low cost is pursued by using a 0.35 μm CMOS technology without RF options, and by using an inductorless circuit topology which leads to a final active area of $190 \times 180 \mu\text{m}^2$ for the complete LNA, which is in the order of the area of a single inductor. The LNA exhibits a voltage gain of 15 dB, a S_{11} below -10dB and a noise figure under 3 dB in a 1 GHz band. The power consumption is 12.4 mW from a 1.8 V voltage supply.

Keywords— Wideband, Inductorless, Low Area, Low Cost, Low Noise Amplifier.

I. INTRODUCTION

Many applications do not need to have a standard compliant radio link: they just require a very simple, low-data rate radio link, which can be implemented with reduced circuit complexity, with low area and low power. Low-cost is a key feature for non-critical applications especially when referring to disposable units. These applications are often implemented in the Instrumental, Scientific and Medical (ISM) bands. The bands of 433.05–434.79 MHz and 902–928 MHz (depending on bandwidth and region, as these are non-universal bands) are most used as they lead to an interesting trade-off for implementation cost and path loss attenuation. These frequencies also allow the use of a lower cost technology without requiring state-of-the-art nanoscale technologies.

The approach to realize low-cost RF circuits in a mainstream digital process (without requiring expensive process options) is to explore inductorless circuits since they provide large savings in area and have the added advantage of being wideband and able to operate in multi-ISM bands if needed.

One building block that commonly requires inductors in a receiver is the LNA. Inductors are good to realize tuned narrowband LNAs with low noise [1, 2]. Ideal inductors do not generate noise; however in practice they generate it due to their parasitic coil resistance. Inductors can also be found in multi-band and wideband LNAs [3-5]. One disadvantage of inductors is their large area in comparison with other circuit elements [2]. Recently, work on inductorless LNAs design with noise reduction has been addressed [6].

In this paper we present an inductorless low noise amplifier (LNA) designed to be used in receivers for sub-GHz ISM bands using a standard 0.35 μm digital CMOS technology, without requiring RF options such as thick copper top metal layer for inductor implementation. For the wanted frequency bands and the transistor f_T values, it is possible to use feedback techniques. The LNA proposed here is a shunt-shunt feedback amplifier similar to that presented in [7] adapted to single-ended version and having other changes to further reduce the area, without sacrificing the performance. Most recently, in [8] were also presented LNA topologies close to the topology under study here.

In an LNA design there is a trade-off between its main specifications [9], being the most relevant, and the ones studied here, the input impedance matching (usually 50 Ω), the gain, and the noise figure. The feedback topology allows obtaining these in an almost independent way providing extra design freedom.

This paper also presents the analysis of the shunt-shunt feedback topology applied to this particular circuit using the blocks admittance matrices which proves to be a very useful approach to obtain insight and usable guidelines for the circuit dimensioning.

This paper is organized as follows. In section II we present the low noise amplifier circuit and describe its' functionality. In section III we present a small signal analysis of the circuit and we determine the expressions for the input impedance and for the gain. A first dimensioning for the circuit is derived. In section IV we present simulation results and the layout. Finally, in section V we draw some conclusions.

II. CIRCUIT DESCRIPTION

The proposed low noise amplifier is presented in figure 1. The circuit can be divided in two main blocks: the amplifying block (M_1 , M_4 and R_D) and the feedback block (M_2 and R_1), being M_3 and M_5 accessory elements, important for biasing and for the circuit performance as it will be explained.

The amplifier stage is a cascode stage with a resistive load, where both transistors M_1 and M_4 must operate in the saturation region. The gain of such a stage depends mainly on

the g_{m1} and on the R_D value as it is in first order approximation given by the product $g_{m1}R_D$. A high g_{m1} requires high current but such a high current causes a high voltage drop in R_D , and then M_1 and M_4 are no longer in the saturation region. This limits the resistor R_D value, limiting the circuit gain. To solve this limitation current steering is used via transistor M_5 . It is now possible to provide the necessary current to transistor M_1 and obtain a higher g_{m1} , and simultaneously avoid the unnecessary high voltage drop in R_D leaving its common-mode voltage closer to V_{DD} .

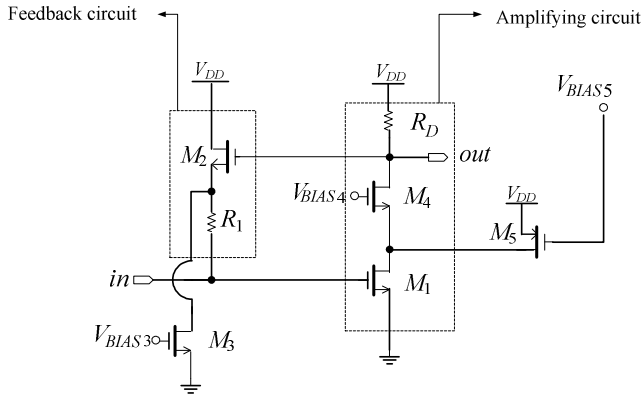


Figure 1 – Wideband inductorless low noise amplifier.

The feedback block, built with M_2 and resistor R_1 , is suitable to achieve the 50Ω input match. Therefore the gain and the input impedance can be obtained without compromise as desired. The common-source transistor M_3 is used to permit the biasing of M_2 without causing the voltage drop in R_1 . This allows the direct connection of M_2 to the output node without requiring an AC-coupling as in [7] saving the area required for the bias resistor and the large coupling capacitor.

In the following section a more detailed circuit analysis is performed.

III. OVERALL GAIN AND INPUT IMPEDANCE

This LNA is a shunt-shunt feedback amplifier, since it samples the output voltage and compares current at the input [10]. This feedback topology is represented in figure 2.

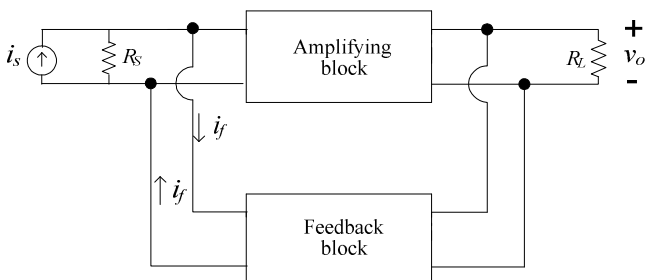


Figure 2 – Shunt-shunt feedback topology.

The amplifying block, the feedback block and the complete circuit can all be represented by the diport

admittance matrix (1) and the equivalent circuit represented in figure 3.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (1)$$

In the shunt-shunt topology, the admittance matrix representing the complete circuit can be easily obtained by simply adding the admittance matrices of the amplifying block and feedback block [11].

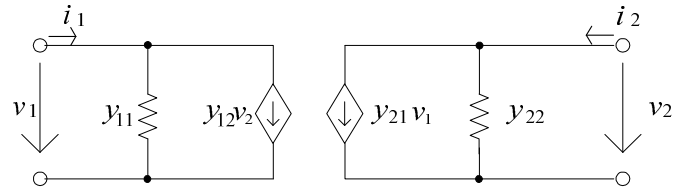


Figure 3 – Diport equivalent circuit using the admittance matrix elements.

The amplifying block and the feedback block must be identified in the proposed circuit. As represented in figure 1, the amplifying block is composed by transistors M_1 , M_4 , and the load resistor R_D . The feedback block includes the common drain transistor M_2 and the resistor R_1 . The biasing and the current steering blocks are considered ideal and therefore are excluded from this small-signal analysis.

The amplifying block consists on a cascode stage. Considering that the output impedance is dominated by R_D , which is much smaller than $g_{m4}r_{o4}r_{o1}$, its small-signal circuit can be simplified to the one represented in figure 4 where the input transistor M_1 contributes with the input capacitance and the circuit g_m (in the cascode topology the input-output capacitance can be neglected) while R_D is responsible for the circuit output impedance.

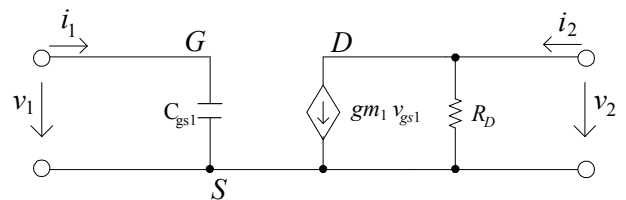


Figure 4 – Simplified small-signal circuit of the amplifying block.

The \mathbf{Y} -parameters for the amplifying block are:

$$\begin{cases} y_{11A} = sC_{gs1} \\ y_{12A} = 0 \\ y_{21A} = g_{m1} \\ y_{22A} = \frac{1}{R_D} \end{cases} \quad (2)$$

The small-signal circuit of the feedback block is represented in figure 5:

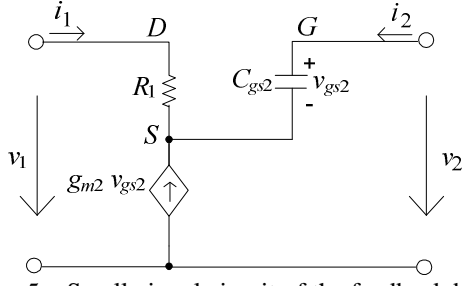


Figure 5 – Small-signal circuit of the feedback block.

The Y-parameters for the feedback block are:

$$\left\{ \begin{array}{l} y_{11\beta} = \frac{sC_{gs2} + g_{m2}}{(1 + R_1 \cdot g_{m2} + R_1 \cdot sC_{gs2})} \\ y_{12\beta} = -\frac{sC_{gs2} + g_{m2}}{(1 + R_1 \cdot g_{m2} + R_1 \cdot sC_{gs2})} \\ y_{21\beta} = -\frac{sC_{gs2}}{(1 + R_1 \cdot g_{m2} + R_1 \cdot sC_{gs2})} \\ y_{22\beta} = \frac{sC_{gs2}}{(1 + R_1 \cdot g_{m2} + R_1 \cdot sC_{gs2})} \end{array} \right. \quad (3)$$

To obtain the LNA equivalent Y-parameters, the Y-matrices of both blocks, (2) and (3), are summed:

$$\left\{ \begin{array}{l} y_{11} = y_{11A} + y_{11\beta} = sC_{gs1} + \frac{sC_{gs2} + g_{m2}}{(1 + R_1 \cdot g_{m2} + R_1 \cdot sC_{gs2})} \\ y_{12} = y_{12A} + y_{12\beta} = -\frac{sC_{gs2} + g_{m2}}{(1 + R_1 \cdot g_{m2} + R_1 \cdot sC_{gs2})} \\ y_{21} = y_{21A} + y_{21\beta} = g_{m1} - \frac{sC_{gs2}}{(1 + R_1 \cdot g_{m2} + R_1 \cdot sC_{gs2})} \\ y_{22} = y_{22A} + y_{22\beta} = \frac{1}{R_D} + \frac{sC_{gs2}}{(1 + R_1 \cdot g_{m2} + R_1 \cdot sC_{gs2})} \end{array} \right. \quad (4)$$

The voltage gain (A_v) and the input impedance (Z_{in}) are obtained by the following expressions [5]:

$$\begin{aligned} A_v &= -\frac{y_{21}}{y_{22} + G_L} = \\ &= -\frac{g_{m1} \cdot R_D \cdot (1 + g_{m2} \cdot R_1 + sC_{gs2} \cdot R_1) - sC_{gs2} R_D}{1 + g_{m2} \cdot R_1 + sC_{gs2} \cdot (R_1 + R_D)} \end{aligned} \quad (5)$$

$$\begin{aligned} Z_{in} &= \left(y_{11} - \frac{y_{12} \cdot y_{21}}{y_{22} + G_L} \right)^{-1} = \\ &= \frac{1 + g_{m2} \cdot R_1 + sC_{gs2} \cdot (R_1 + R_D)}{g_{m2} (1 + g_{m1} \cdot R_D) + sC_{gs1} \cdot (1 + g_{m2} \cdot R_1 + sC_{gs2} \cdot (R_1 + R_D)) + sC_{gs2} (1 + g_{m1} R_D)} \end{aligned} \quad (6)$$

If the transistors' C_{gs} effect is neglected, the voltage gain and the input impedance simplifies to the passing band known results as expected:

$$A_v = -\frac{g_{m1} \cdot R_D \cdot (1 + g_{m2} \cdot R_1)}{1 + g_{m2} \cdot R_1} \approx -g_{m1} \cdot R_D \quad (7)$$

$$Z_{in} = \frac{1 + g_{m2} \cdot R_1}{g_{m2} (1 + g_{m1} \cdot R_D)} \approx \frac{1 + g_{m2} \cdot R_1}{g_{m2} \cdot (1 + |A_v|)} \quad (8)$$

Expressions (7) and (8) are used to obtain a first draft of the circuit dimensioning for the passing band as they neglect high frequency effects. Expressions (5) and (6) are then used to dimension the circuit according to the wanted bandwidth as they determine the input impedance (S_{11}) adapted band.

Expressions (5) to (8) also indicate dimensioning trade-offs that can be summarized as:

- g_{m1} and R_D determine the LNA gain:
 - A higher g_{m1} can be obtained either by increasing the W/L ratio of the transistor M_1 , or by increasing its drain current. Increasing W/L increases C_{gs1} and increasing the drain current penalizes the LNA power consumption;
 - A higher R_D leads to a high voltage drop at the resistance, which can take transistors out of the saturation region, increases noise and reduces the bandwidth.
- g_{m2} and R_1 determines predominantly the input impedance.

To determine a first circuit dimensioning we use expressions (5) to (8), aiming a constant value of the voltage gain of about 20 dB and input impedance of 50 Ω till 2 GHz, to ensure that after the implementation we have a voltage gain of at least 15 dB within 1 GHz bandwidth. We assume a voltage drop at R_D of 400 mV (for a voltage supply value of 1.8 V, it leaves 1.4 V for transistors M_1 and M_4). Reasonable values are a 2 mA current on a 200 Ω resistor. To have 20 dB of voltage gain, g_{m1} becomes 50 mS. As a trade-off to lower the power consumption and the transistor size, still having an effective feedback factor, leded to consider a g_{m2} five times smaller than g_{m1} . The remaining parameters are calculated from (5) and (6) using a numerical program. The obtained results can be used to evaluate the circuit feasibility within the implementing technology.

In Table I the values used as a first draft for the circuit dimensioning are listed.

Table I – Parameters used for the first dimensioning.

Parameter	Value
$C_{gs1} = C_{gs2}$	400 fF
R_1	350 Ω
R_D	200 Ω
g_{m1}	50 mS
g_{m2}	10 mS

The expected results from (5) and (6) using the values in Table I are represented in figures 6 and 7. In figure 6 is represented the voltage gain, using expression (5), in figure 7 is represented the S_{11} .

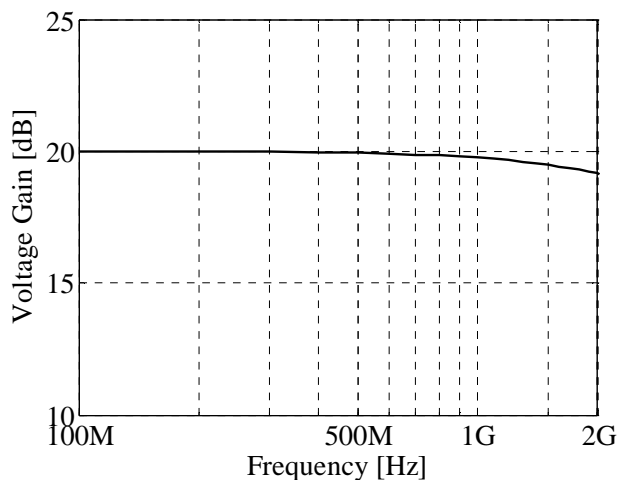
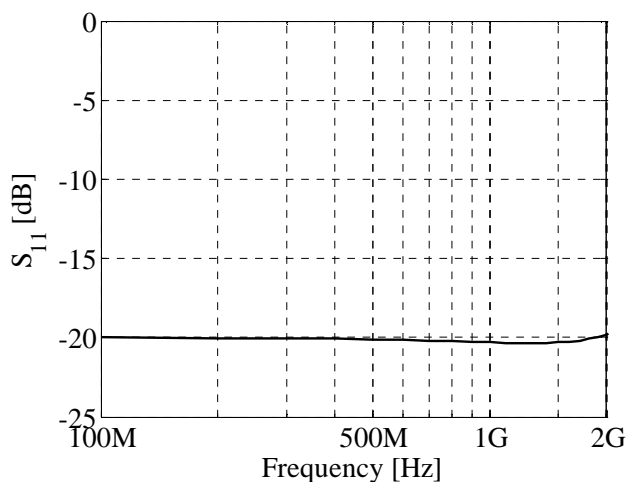


Figure 6 – LNA Voltage gain.

Figure 7 – LNA S_{11} .

Figures 6 and 7 shows that the values considered allow an LNA upper bandwidth limit of approximately 2 GHz. These results use simplified models, thus it is expected that using

real models in a circuit simulator the circuit performance will be deteriorated.

IV. SIMULATION RESULTS

The circuit is implemented in a low-cost 0.35 μ m CMOS technology, using a 1.8 V supply voltage. The values in Table I are used to perform the first LNA transistor dimensioning. This circuit implementation shows that with a 2 mA current for the wanted g_{m1} implies such a large transistor that exceeds the C_{gs} calculated value, reducing considerably the bandwidth. The solution is to use current steering, via transistor M_5 , that does not affect the current in R_D but it ensures the g_{m1} with a smaller transistor. After a few iterations, the sizing that meets the better trade-off between voltage gain, input impedance and noise figure is listed in Table II.

The current flowing through the different circuit elements, the transconductances and the gate-source capacitances of the transistors are listed in Table III. The voltage gain, the S_{11} and the noise figure obtained are represented in figures 10 to 12.

Table II – Final circuit dimensioning.

Parameter	Value
$(W)_1[\mu\text{m}]$	500
$(W)_2[\mu\text{m}]$	250
$(W)_3[\mu\text{m}]$	10
$(W)_4[\mu\text{m}]$	150
$(W)_5[\mu\text{m}]$	100
$(L)_{1-5}[\mu\text{m}]$	0.35
$R_D[\Omega]$	120
$R_1[\Omega]$	230

The first observation is that the upper limit of the LNA bandwidth has dropped, mainly due to S_{11} , which is only below -10 dB till approximately 1 GHz. The voltage gain also reduces, in comparison with that expected, mainly due to the reduction of R_D . R_D has to be kept low due to its influence on the noise figure which we try to keep below 3 dB until 1 GHz. This value is in accordance with typical LNA noise figure values. The circuit consumes 12.4 mW from a 1.8 V voltage supply.

Table III – Biasing and small signal parameters (current, transconductance and gate-source capacitance).

Element	I [mA]	g_m [mS]	C_{gs} [fF]
M_1	6.5	57.4	463.9
M_2	0.4	9.6	206.8
M_3	0.4	1.6	9.3
M_4	2.1	17.5	138.7
M_5	4.5	7.8	109.7
R_D	2.1	-	-
R_1	0	-	-

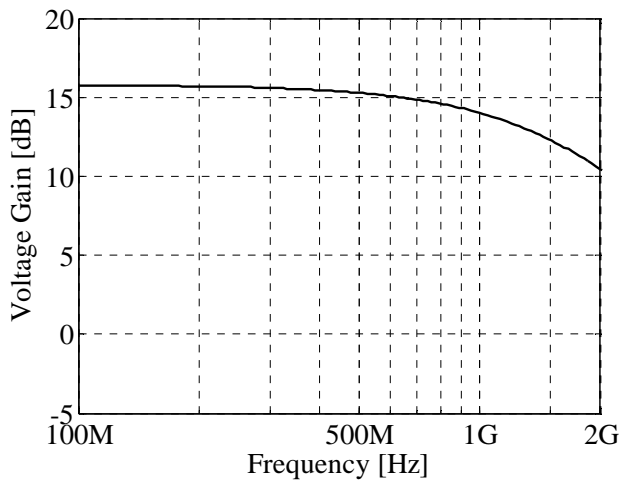


Figure 10 – LNA Voltage gain.

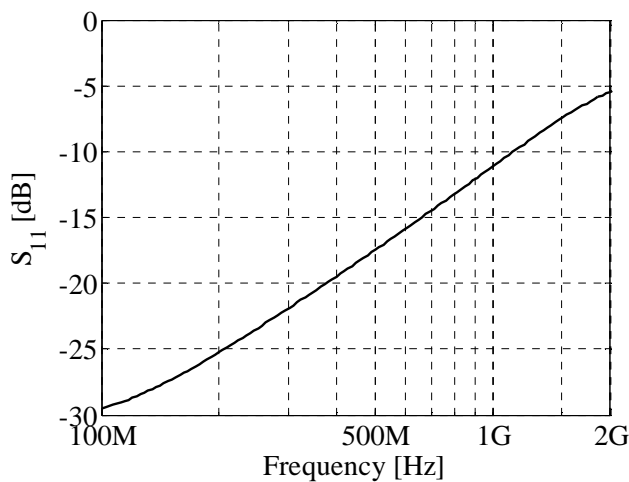
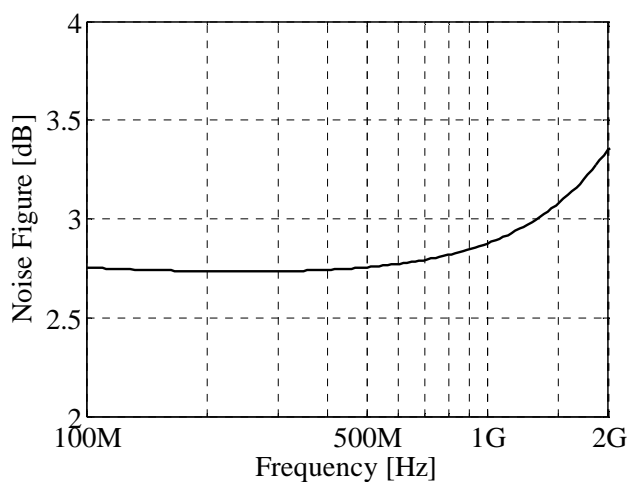
Figure 11 –LNA S_{11} .

Figure 12 –LNA noise figure.

In figure 13 is represented the circuit layout, where the active area (excluding pads and decoupling capacitors) is only $190 \times 180 \mu\text{m}^2$.

Special attention is taken for the layout to the following aspects:

- several pads are used for both V_{DD} and GND to minimize the parasitic inductances of the bonding pads;
- decoupling capacitors and a ground plane on chip are used to mitigate on chip parasitic inductances due to wiring and ensure stable on-chip power supply values;
- all connections inside the LNA are small and straight to avoid current loops and to minimize parasitic inductances;
- all devices have a guard ring to improve the substrate biasing and reduce noise;
- input and output pads are smaller to reduce their parasitic capacitances;
- all lines are designed to support a current higher than expected.

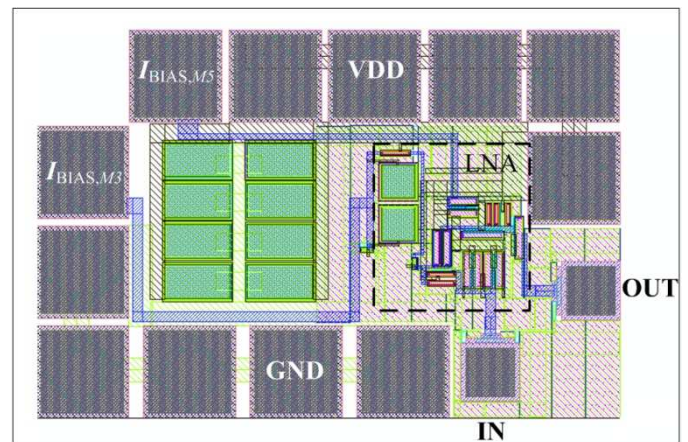


Figure 13 – LNA layout.

V. CONCLUSIONS

In this paper we present a design procedure for the dimensioning of an inductorless LNA. The LNA under study has a shunt-shunt feedback topology and it is studied using the admittance-matrix approach which leads to useful expressions for the voltage gain and input impedance. This approach allowed the change of a known LNA topology into a simpler version without large capacitors which together with the absence of inductors leads to a final circuit with an active area of just $190 \times 180 \mu\text{m}^2$. The LNA performance is within reasonable values for the intended low-cost, non-critical, applications; it has a voltage gain of 15 dB, an S_{11} smaller than -10dB and a noise figure below 3 dB up to 1 GHz, covering two ISM bands. The power consumption is 12.4 mW at a 1.8 V voltage supply.

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