Design of a 1 Gb Radiation Hardened NAND Flash Memory

Nikhil Gupta, Bert Vermeire, Hugh Barnaby
Department of Electrical Engineering
Arizona State University
Tempe, USA

Murat Goksel, Edward Li, David Czajkowski
Space Micro Inc.
San Diego, USA

Abstract – **Non-volatile memories used in the space environment typically require radiation hardened process technologies. These technologies are not only costly, but the resultant die occupies more area compared to commercial memories of comparable size. This in turn limits the memory density of these radiation hardened memories. In this paper, we present a technique for the development of a low cost 1 Gb radiation hardened (Rad Hard) NAND flash memory manufactured with commercial components. The design methodology provides an alternate strategy for producing radiation hardened memory while simultaneously achieving higher cell densities at lower costs.**

Keywords – SEU, SEFI, Rad Hard, COTS, TMR, EDAC

I. INTRODUCTION

Non-volatile memory devices available for use in the harsh radiation environment of space are confined to relatively small EEPROM devices. These devices make use of specialized process technologies that are radiation hardened. These special process technologies [1] [2] are expensive and are typically a few generations behind commercial processes. Moreover, the resultant radiation hardened memory cell area is larger than the cell area of a commercial memory. As a result, the memory capacity of these hardened devices is limited to a few Mb.

Existing high density commercial flash memories can not be used in space applications because of their low radiation tolerance. Even as process technology scaling for commercial flash memories improve total ionizing dose (TID) and single event latchup (SEL) tolerance, the same process changes generally increase device susceptibility to single event upsets (SEUs) and single event functional interrupts (SEFIs).

The use of commercial-off-the-shelf (COTS) parts for space applications has been a subject of discussion [5]. If a COTS flash memory could be used for space applications, it would greatly reduce the cost while significantly increasing memory density. In order for COTS memories to be used in space, a method must be devised to mitigate the radiation effects. In this paper, we present a combination of hardening strategies that can be applied to a COTS memory to render it useful in a radiation environment. First, we discuss the advantages and disadvantages of using a COTS memory and then describe techniques to overcome these disadvantages. We then present results that demonstrate the viability of the methodology.

II. ADVANTAGES OF USING A COTS PART

A. Lower cost associated with a COTS Component

The cost of a commercial part can be a fraction of its radiation hardened counterpart. As explained earlier, this is in part due to the advanced process technologies that are used for manufacturing radiation hardened memories. Popular radiation hardening by process (RHP) technologies include silicon oxide nitride oxide semiconductor (SONOS) technology [3] and RH25, a radiation hardened CMOS technology [4]. In addition, the development of a new radiation hardened component using RHP requires the designer to go through the entire ASIC development flow. This involves non-recurrent engineering (NRE) costs such as development of masks for fabrication which can be quite expensive [5] [6]. Commercially manufactured parts, on the other hand, are developed on a very large scale for a variety of applications and hence the NRE costs are divided over a greater volume of finished parts. As a result, these COTS parts are significantly cheaper than their radiation hardened counterparts.

B. Shorter Development Time

The ASIC development flow described above not only costs more, it also increases development time compared to the use of a COTS part directly in a radiation hardened system [5].

C. Use of Latest Technology

The feature size of the devices used in commercially available parts is several generations ahead of that used in components that are intrinsically radiation hardened. The use of the latest technologies and the smaller feature size of commercial parts leads to better performance and higher cell densities, compared to their radiation hardened counterparts [5].

III. DISADVANTAGE OF USING COTS PART

A. Radiation Effects in COTS Parts

COTS parts are not designed for the radiation environment. They suffer from single event upsets, single event functional interrupts and even permanent damage in space [5]. These radiation effects produce soft errors or can cause the COTS part to stop responding either temporarily or permanently. This behavior can be critical in space missions where, once these parts stop functioning, replacing them can be difficult if not impossible. The soft errors induced due to SEUs can be reduced by the use of silicon-on-insulator (SOI) technology.

However, even if the COTS parts can be protected from SEUs, they may still remain susceptible to SEFIs [5].

B. *Short Life Cycle associated with a COTS Components*

The COTS market is highly dynamic and the average life cycle for a COTS part is very small compared to a radiation hardened part. For a COTS component, a new, more advanced product is launched every 2 to 3 years, while radiation hardened components may have a life cycle of 15 years [6]. This short life cycle is attributed largely to the highly competitive commercial market [5] and is a major problem when it comes to choosing a commercial part for radiation hardened applications. One must make sure that the component will be available in some form over an extended period of time, even if it becomes "obsolete" in terms of its use in commercial applications. One option to solve this issue is to buy the intellectual property for this COTS part. But this can be expensive and reduces some of the advantages gained by the use of a commercial product [5]. A better option is to design the radiation hardened system in such a manner that it can use COTS parts that are available today, as well as newer COTS parts that will be available in the future.

IV. Radition Effects in COTS NAND Flash Memories

Several flash memories have been tested to characterize their radiation response [7], "unpublished" [8]. Of these, a 2 Gb Micron NAND flash memory was found to be reasonably tolerant to radiation and were deemed suitable for certain space applications [7]. We are briefly going to describe these findings for this Micron NAND flash memory.

A. *Single Event Upsets (SEU)*

Single event upsets of the memory cells results in the change of the value stored in the cell from logic '0' to logic '1'. SEU is caused due to the interaction between an ion and the floating gate of a memory cell. The data in the memory cell is stored in the form of presence or absence of electrons in the floating gate. Logic '0' is stored as the presence of electrons and logic '1' is stored as the absence of electrons. When an ion interacts with a memory cell storing logic '0', it neutralizes the charge due to electrons and causes the bit to flip to logic '1'. The tests conducted in [7] found the number of single bit errors induced in the memory to be reasonably low. The result of this study has been re-plotted in Figure 1 for the dynamic read/write test. The y-axis on the left side represents the cross-section for SEU. It is normalized to a single ion. Therefore, when a single ion is exposed to 1 cm^2 of the chip area, the cross-section represents the critical area it must pass through in order to cause a SEU (single bit error). Hence, the cross-section is the probability that an ion passing through that cm^2 causes a SEU.

B. *Single Event Functional Interrupts (SEFI)*

SEFIs are caused by the interaction of an ion with the control logic in a memory. This may lead to multiple bit errors (page or block errors) in a memory or cause the memory to stop responding temporarily until it is restarted (power on that memory part is cycled off/on). The tests conducted in [7] found that the Micron memory is susceptible to SEFIs. The result of this study has been re-plotted in Figure 1 for the dynamic read/write test. The y-axis on the right side represents the cross-section for SEFI. It is normalized to a single ion. Therefore, when a single ion is exposed to 1 cm^2 of the chip area, the cross-section represents the critical area it must pass through in order to cause a SEFI in the device. Hence, the cross-section is the probability that an ion passing through that cm^2 causes a SEFI.

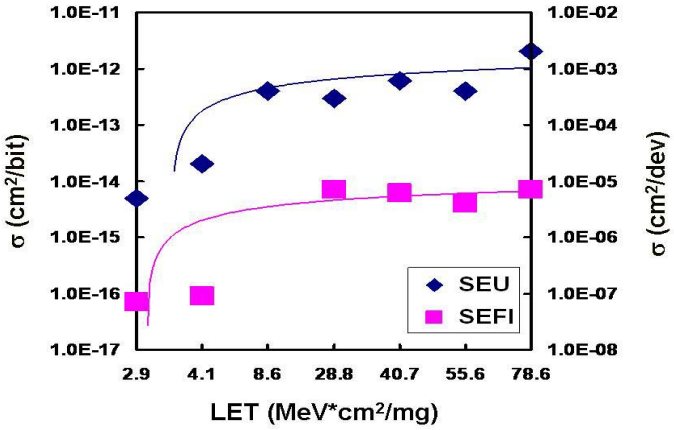

Figure 1: SEU and SEFI cross-section for a 2 Gb Micron NAND Flash memory without mitigation

V. Overcoming the Disadvantages of Using COTS Memory

A. *Mitigating the radiation effects on the Flash Memory*

In this paper, we present a combination of radiation hardening strategies that, when applied on this Micron NAND flash memory, can improve its resistance to SEUs and harden it against SEFIs. This strategy is general and can be applied to other COTS NAND flash memories also.

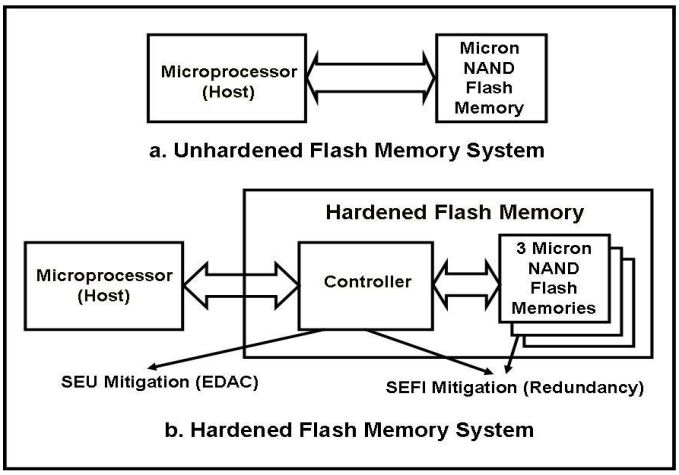

Figure 2: The unhardened and the hardened flash memory system

The method we propose to address SEUs and SEFIs is to use triple module redundancy (TMR) at the system level combined with error detection and correction (EDAC) at the memory level. This strategy is implemented in a memory controller which acts like an interface between the microprocessor and the Micron NAND flash memories used in the hardened flash memory (Figure 2). In TMR, redundancy is

introduced in the system by using three identical COTS memories. If one of the memories fails to respond due to SEFI, then the other two memories can be used to fetch the correct data.

SEU mitigation is addressed by adding EDAC to each memory. EDAC can correct bit errors caused by SEU. We evaluated a number of EDAC codes and found Hamming codes with the capability of detecting two errors and correcting one error to be the most suitable for our system.

To cause a SEFI in the hardened flash memory, an ion must cause a SEFI in all three memories. Also, to cause a SEU in the hardened flash memory, an ion must cause a SEFI in two of the three memories and cause a 2 bit error in the third memory. In that case, a combination of TMR and EDAC will not be able to retrieve the correct data from the memories. The cross-section for SEU and SEFI with mitigation has been plotted in Figure 3 for the same dynamic read/write test as in Figure 1. It can be seen that the probability of an ion causing a SEU or SEFI in the hardened flash memory is considerably lower compared to an unhardened COTS memory.

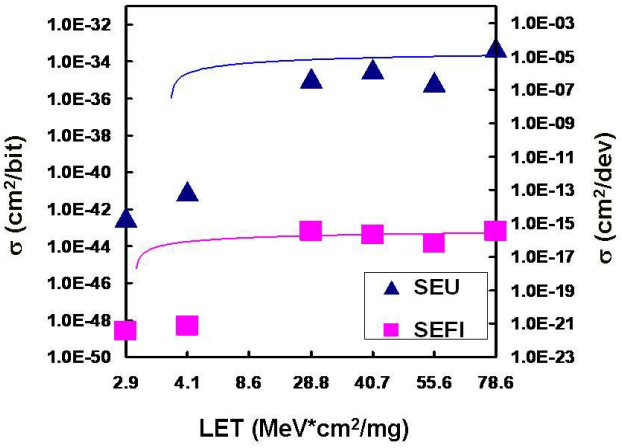

Figure 3: SEU and SEFI cross-section for a 2 Gb Micron NAND Flash memory with mitigation

For the COTS memory, the number of bit errors per bit read is the sum of the bit errors due to SEFI and due to SEU. For a space mission, the error rate will depend on the prevalence of particles as a function of LET. We have considered a LET of 4.1 MeV*cm^2/mg for a sample calculation to illustrate the amount of hardening achieved by using the combination of TMR and EDAC. We assume that it takes 10 msec to detect a SEFI, power down the memory, and power it up again. We also assume that the particle flux in orbit is 100 particles/cm^2-day. From Figure 1, we find that the probability that a single particle per unit area with a LET of 4.1 MeV*cm^2/mg will cause a SEFI is 9 x 10^{-8}. Therefore, the number of SEFIs caused in a day is given by the following equation:

Number of SEFIs per day = Probability that 1 particle passing per unit area will cause a SEFI * Particle flux (1)

From (1), we find that the number of SEFIs per day is 9 x 10^{-6}. The probability that the memory is unavailable at any given instant of time is given by the following equation:

Probability that a memory is unavailable = Number of SEFIs per day * Time taken to detect a SEFI in a memory and restart the memory / Duration of one day (2)

From (2), we find that the probability that a memory is unavailable due to SEFI is 1.04*10^{-12}. For SEUs, the probability that a bit will be read incorrectly is the product of the cross-section and particle fluence.

For the hardened system, the number of bit errors per bit read is a sum of the bit errors of 4 cases:

Case 1: All 3 memories suffer from SEFI

Case 2: 2 memories suffer from SEFI and 1 from SEU

Case 3: 1 memory suffers from SEFI and 2 from SEU

Case 4: All 3 memories suffer from SEU

The results have been plotted in figure 4. It can be seen that the number of bit errors per bit read is lower in the hardened flash memory than in the unhardened COTS memory by several orders of magnitude.

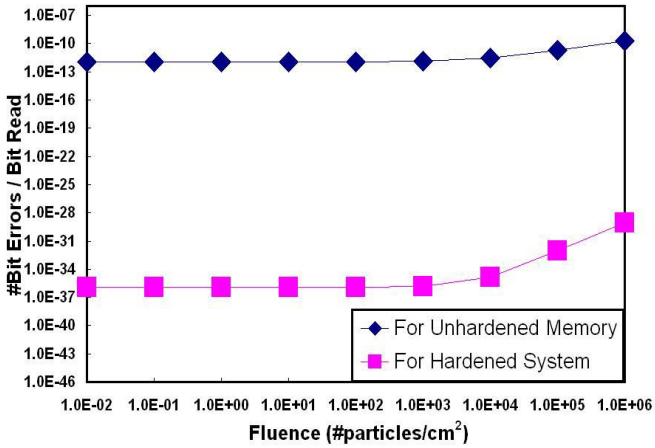

Figure 4: Number of bit errors per bit read as a function of particle fluence for a LET of 4.1 MeV*cm^2/mg

B. *Making the system scalable*

In order to make the hardened flash memory compatible with future generations of COTS memories, we ensured that our hardening strategy was fairly general and did not make use of any special characteristic of the Micron NAND Flash such as its page size. This makes this strategy scalable with memory size.

The hardened flash memory is also designed to preserve the standard interface between a microprocessor (host) and a COTS flash memory. Although, the hardened flash memory described in this paper uses NAND flash memories internally, it can be interfaced to the microprocessor with either a NAND flash or a NOR flash interface. Therefore, the commands issued from the microprocessor to the hardened flash memory can either be the standard NAND flash or the standard NOR flash commands. This increases the versatility of the hardened flash memory.

VI. TEST SETUP

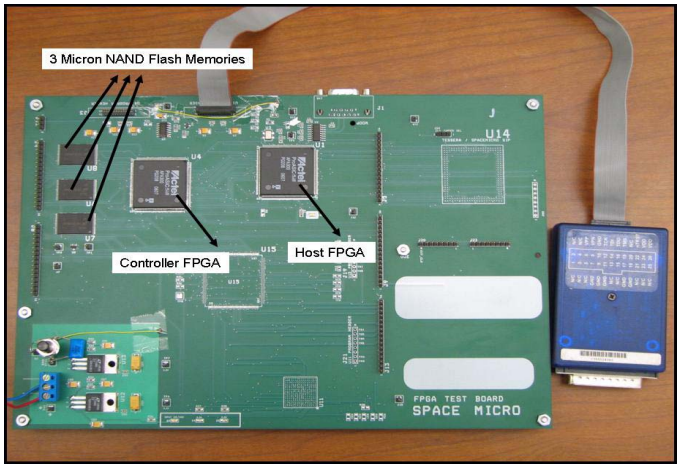

Figure 5: Test Board

Figure 5 shows the test setup built for testing the hardened flash memory. It consists of two FPGA's. One FPGA is used to imitate the microprocessor (host) that will issue the commands to the hardened flash memory. The second FPGA is for the controller on which the actual radiation hardening strategy (TMR and EDAC) will be implemented. As seen in Figure 5, there are 3 NAND Flash memories which form a part of the Triple Module Redundancy block.

VII. RESULTS

The functionality of the hardened flash memory has been verified. The results are shown in this section. For all the results shown, the microprocessor (host) issues instructions to the controller in the standard NOR instruction format. The instructions from the controller to the 3 memories are always issued in the NAND format since these memories are NAND flash memories.

Figures 6 and 7 depict the erase operation in the hardened flash memory. Figure 6 shows the host issuing the erase command to the controller in the NOR format. The controller decodes the instruction and issues the same command in the NAND format to the three memories on lines ioa, iob and ioc. This is shown in Figure 7.

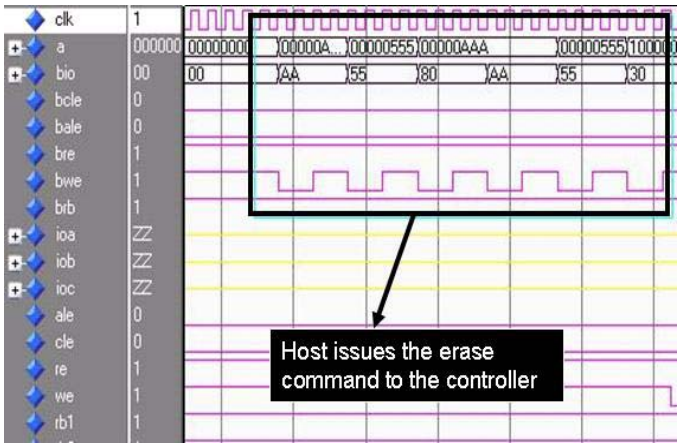

Figure 6: Host issues the erase command to the controller

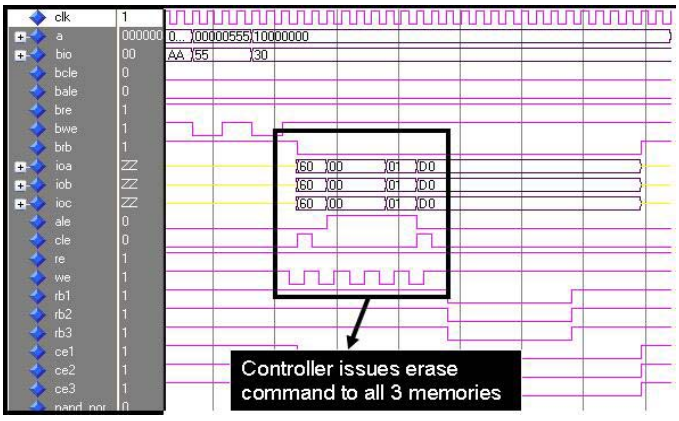

Figure 7: The controller issues the Erase command to all 3 memories

Figures 8, 9 and 10 show the write operation in the hardened flash memory. The host issues the write command to the controller in the NOR format (Figure 8). The controller decodes this instruction and issues the write command to the three memories in the NAND format (Figure 9). EDAC is added to the data before it is send to these memories. For every byte of data from the host, the controller will send 2 bytes of data to each of the three memories. These two bytes include the original data along with the interleaved parity bits. This is shown in Figure 10. The byte CC from the host to the controller is represented as 6A and 0C from the controller to the three memories. Similarly, byte DD from the host to the controller is represented as bytes EC and 0D from the controller to the three memories.

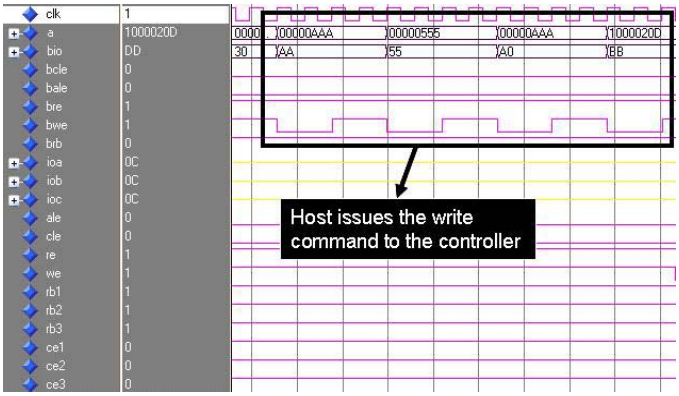

Figure 8: Host issues the write command to the controller

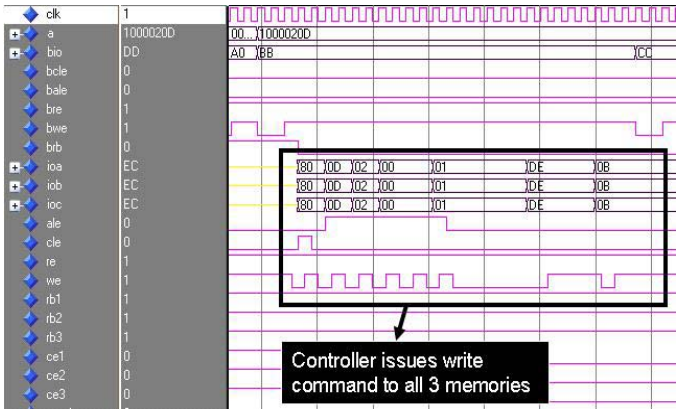

Figure 9: Controller issues the write command to the 3 memories

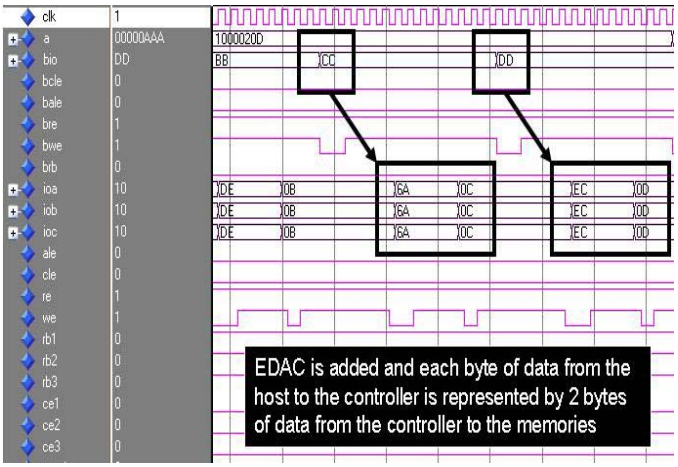

Figure 10: EDAC is added to the data that has to be written to the memories

Figure 11 and 12 demonstrate the read operation in the hardened flash memory. The host issues a read instruction to the controller in the NOR format. The controller decodes this instruction and issues the read command to the 3 memories in the NAND format. This can be seen in Figure 11. The data fetched from the three memories (Figure 12) consists of the original data and the interleaved parity bits. Some of the memories may suffer from SEU or SEFI. In this example, Memory A suffers from SEU which causes a single bit flip. Hence 6A and 0C is represented as 6A and 04. Memory C suffers from multiple bit errors due to SEFI. This is represented as all zeros. Memory B does not have either SEFI or SEU. It can be seen that even though Memory A suffers from SEU and Memory C from SEFI, the controller can still decode the correct data (CC) and send it back to the host (Figure 12). These results demonstrate that this controller is able to mitigate the effects of SEU and SEFI in this Micron NAND flash memory.

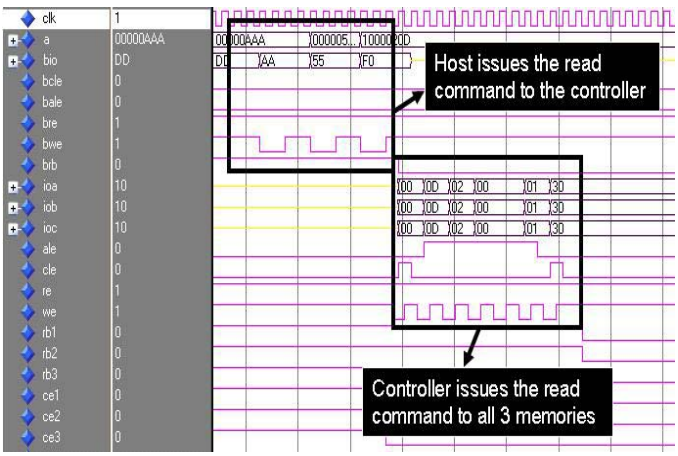

Figure 11: Read command from the host to the controller and from the controller to the 3 NAND flash memories

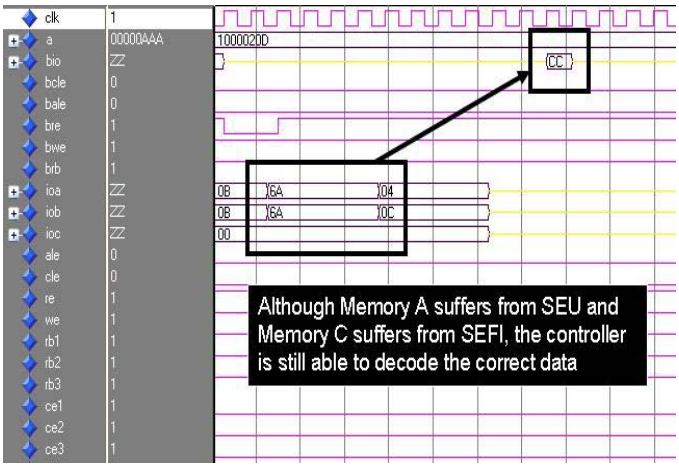

Figure 12: The controller can decode the correct data even if one memory suffers from SEFI and another from SEU.

VIII. Conclusion

Radiation hardened memories that are dependent on process technologies are expensive and are limited to a few Mbs. Multiple COTS Flash memories can be combined into a single hardened flash memory in which, the radiation effects are properly mitigated using TMR and EDAC. This technology will make large flash memories available to space systems at significantly lower cost than available today.

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