Design of Quaternary Logic gate Using Double Pass-transistor Logic with neuron MOS Down Literal Circuit

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Abstract

A multi-valued logic(MVL) pass gate is an important element to configure multi-valued logic. Multiple logical levels which are different from binary pass gates are required to be discriminated in MVL pass gates[1]. In this paper, we designed the Quaternary MIN(QMIN)/negated MIN(QNMIN) gate, the Quaternary MAX(QMAX)/negated MAX(QNMAX) gate using double pass-transistor logic(DPL) with neuron MOS(νMOS) threshold gate. And also we designed Quaternary Truncated Sum(QTS) and Quaternary Truncated Difference(QTD) gate using νMOS down literal circuit(DLC). DPL is improved the gate speed without increasing the input capacitance. It has a symmetrical arrangement and double-transmission characteristics. The threshold gates are composed by νMOS DLC. The proposed gates get the valued to realize various multi threshold voltages. In this paper, these circuits are used 3V power supply voltage and parameter of 0.35um N-Well 2-poly 4-metal CMOS technology, and also represented HSPICE simulation results.

I. INTRODUCTION

There are two kinds of MVL has generally used one of them, voltage-mod MVL circuits have the advantage of low power consumption[1]. But since they require the multi-level ion implantation process technology to realize multi-threshold voltages in MOS transistors, complex fabrication and high cost are inevitable. In order to solve these problems, we try to use a general CMOS process to realize voltage-mode MVL circuits. A pass gate is a popular way to realize a MVL function. The algorithm for simplification of pass gate has already been developed. With the development of MVL theory, the need for MVL circuit design is increased[2].

A neuron-MOS(νMOS) is a kind of novel transistor device with multi-input gates. The νMOS is characterized by a variable threshold voltage achieved by controlling the voltages of the multi-input gates[3]. To design voltage-mod MVL circuits, we present a νMOS down literal circuit(DLC) in this paper. νMOS DLC is applied to MVL pass gate as the threshold gate, and the MVL pass gate can be fabricated with the common CMOS process[4].

Double pass-transistor logics(DPL)[5] gain their speed advantage over CMOS due to their high logic functionality. Also DPL has been developed to improve circuit performance at reduced supply voltage. A symmetrical arrangement and the double-transmission characteristics of the DPL gate compensate for the speed degradation due to the usage of both PMOS and NMOS pass transistors.

In this paper, we designed the quaternary logic gate using the DPL with νMOS threshold gate that has multi-threshold voltage. The νMOS threshold gate is designed by using DLC. The quaternary logic gates include the quaternary MIN(QMIN)/negated MIN(QNMIN) and quaternary MAX(QMAX)/negated MAX(QNMAX). And also we designed the quaternary truncated sum(QTS) and quaternary truncated difference(QTD) gate using νMOS DLC.

These proposed gates are confirmed by HSPICE simulations with 0.35um 2-poly 4-metal CMOS technology and 3V power supply voltage.

The νMOS MVL circuits can be realized without the multi-level ion implantation process technology. The ease of fabrication will make MVL circuits more practically.

II. MULTI VALUED LOGIC

A. νMOS

The basic structure of the functional MOS transistor is

Proceedings of the 34th International Symposium on Multiple-Valued Logic (ISMVL'04)
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shown in Fig.1(a). The multi-input gates are capacitively coupled to the floating gate. The terminal voltages and various capacitive coupling coefficients are defined in Fig.1(b), where Φ_F is the floating-gate potential, V_1, V_2,$\cdots$,V_n are the input signal voltages, C_1, C_2,$\cdots$,C_n the capacitive coupling coefficients between the floating gate and each of the input gates, C_0 is the capacitive coupling coefficient between the floating gate and the substrate, and Q_1, Q_2,$\cdots$,Q_n are the stored charges in each of the capacitors. A symbol representing the device is given in Fig. 1(c).

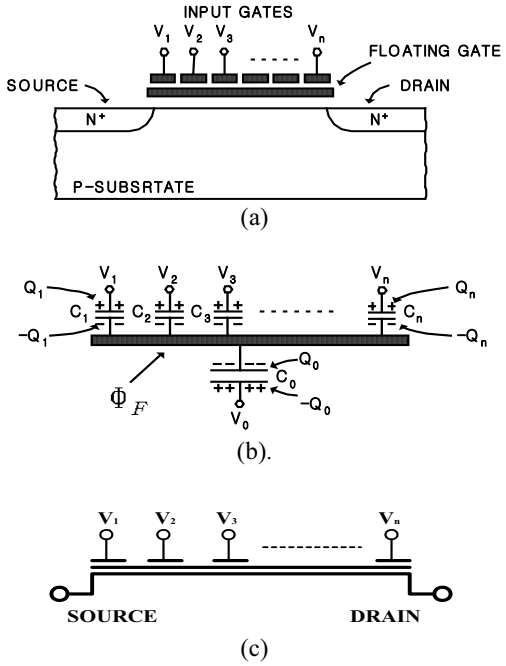


Fig. 1. (a)The basic structure of νMOS. (b)Relationship between terminal voltages and capacitance coupling coefficients. (c)The symbol representing the device.

B. DLC

A DLC is the fundamental element in MVL circuits. MVL logic functions are almost always developed from the down literal function, and most MVL circuits consist of DLC. The down literal function is by Eq.(1).

$$D_i(x) = \begin{pmatrix} R-1 & x \le i \\ 0 & x \ge i+1 \end{pmatrix} \qquad (1)$$

Where, $i \subseteq \{0,1,\cdots,R-2\}$, $x \subseteq \{0,1,\cdots,R-1\}$.

The νMOS DLC consists of p-channel νMOS (νPMOS) and n-channel νMOS (νNMOS) as shown Fig.2.

The common input to νPMOS and νNMOS, V_{in} is taken as the input of the DLC, and V_{b1}, V_{b2} are bias voltages. V_{TC} shown in Eq.(2).

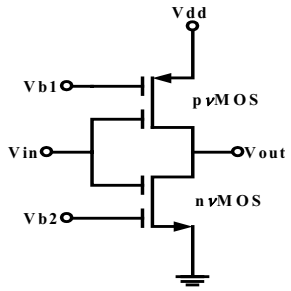


Fig.2. Circuit description of νMOS DLC

$$V_{TC} = V_{DD} - \frac{V_{b1} + V_{b2}}{2} \qquad (2)$$

Here, the restriction of V_{b1}, V_{b2} is derived from saturation condition of νMOS transistors in the circuit. V_{TC} of this circuit can be varied by controlling the values of the bias voltages(V_{b1}, V_{b2}), and different down literal functions can be implemented.

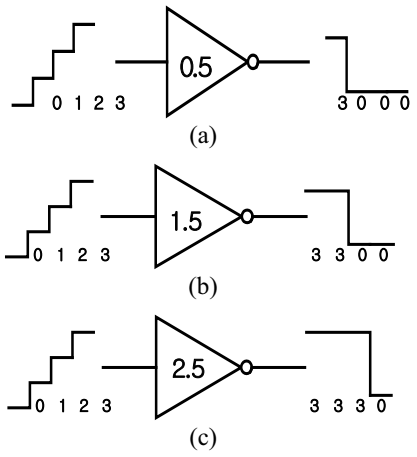
C. Threshold gate

According to Eq.(2), the quaternary DLC can be designed. There are three kinds of down literal functions in the quaternary system. $D_i(x)(i=0,1,2)$ can be attained by setting V_{b1} and V_{b2} to the values stated in Table 1.

Table 1. The transformation of V_{TC} about Bias voltage

V_{DD}=3.3V	V_{TC}	V_{b1}	V_{b2}
V_{th}(0.5)	0.5V	3V	2V
V_{th}(1.5)	1.5V	2.2V	0.8V
V_{th}(1.5)	2.5V	1V	0V

The symbols of the threshold gates are shown in Fig. 3 and also its transfer characteristic of the threshold gates.



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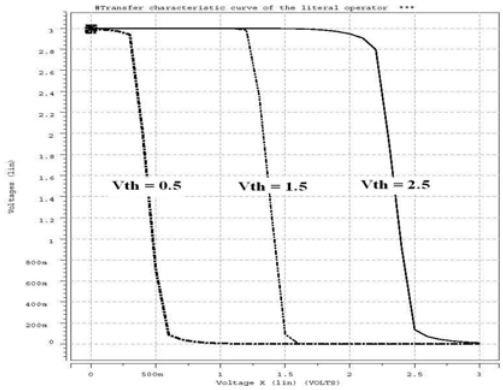


(d)

Fig. 3. (a)V_{th}=0.5 (b)V_{th}=1.5 (c)V_{th}=2.5 (d)Simulation result of transfer characteristic curve

The truth table of quaternary literals is listed in Table 2.

Table 2. The truth table of the quaternary literals

X	X^0	X^1	X^2	X^3	X^{01}	X^{02}	X^{12}	X^{13}	X^{23}	QTS	QTD
0	3	0	0	0	3	3	0	0	0	1	0
1	0	3	0	0	3	3	3	3	0	2	0
2	0	0	3	0	0	3	3	3	3	3	1
3	0	0	0	3	0	0	0	3	3	3	2

D. DPL

Suzuki et al.[5] proposed the DPL that overcomes all the problems of complementary pass-transistor logic(CPL), namely, when implementing CPL, particularly in reduced supply voltage designs, it is important to take into account the problems of noise margins and speed degradation.

DPL consists of both nMOS and pMOS pass transistors, in contrast to CPL. Therefore DPL gives improved circuit performance at reduced supply voltage.

The CPL consists only of nMOS transistors, resulting in low input capacitance and high-speed operation. However, the abovementioned problems are caused by the high output signal level being lower than the supply voltage Vcc by the nMOS threshold voltage Vth. The usual way to avoid this is to use CMOS pass-transistor logic. Full-swing operation is attained by simply adding pMOS transistor in parallel with the nMOS transistors. In the DPL, the inputs to the gates of the pMOS transistor are changed. This arrangement compensates for the speed degradation of CMOS pass-transistors. DPL are symmetrical whereby the load in any DPL is distributed equally among the inputs. This results a balanced input capacitance and reduces the dependence of the delay time on data. Also DPL has double-transmission characteristics[6]. The truth tables in Fig.4 show how the pass transistors operate for the XOR function.

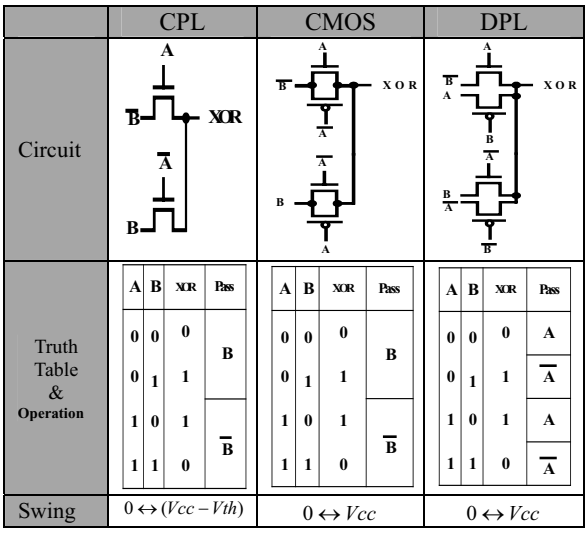


Fig.4. Comparison of CPL, CMOS, and DPL pass-transistor logics for XOR gates

In this table, the column labeled Pass shows which signals are passed and performs the XOR function. As a result, there are always two current paths driving the buffer stage.

III. DESIGN OF QUATERNARY LOGIC GATES

A. QMIN/QNMIN, QMAX/QNMAX

We proposed the QMIN/QNMIN circuit. The QMIN operation is shown as Eq.(3). The operator • or ∧ is QMIN operation.

$$x_1 \bullet x_2 \bullet \cdots \bullet x_n = QMIN(x_1, \cdots, x_n)$$
$$x_1 \wedge x_2 \wedge \cdots \wedge x_n = QMIN(x_1, \cdots, x_n) \quad (3)$$

A QMIN function shown in Table 3 is represented to Eq.(4).

Table 3. QMIN function

B \ A	0	1	2	3
0	0	0	0	0
1	0	1	1	1
2	0	1	2	2
3	0	1	2	3

According to Eq.(4), (5) QMIN and QNMIN can be

easily configured using DPL with νMOS threshold gate.

$$Y = 0 < B^0 > + A < A^{01}, B^{13} > + B < A^{23}, B^{02} > + A < B^3 > \quad (4)$$

$$Y = 3 < B^0 > + \overline{A} < A^{01}, B^{13} > + \overline{B} < A^{23}, B^{02} > + \overline{A} < B^3 > \quad (5)$$

Where Fig.5(b), two input, A and B, are connected in the gate of pass transistor. MOS are turned on or turned off by the input value. Therefore, the output value is generated by QMIN/QNMIN operation.

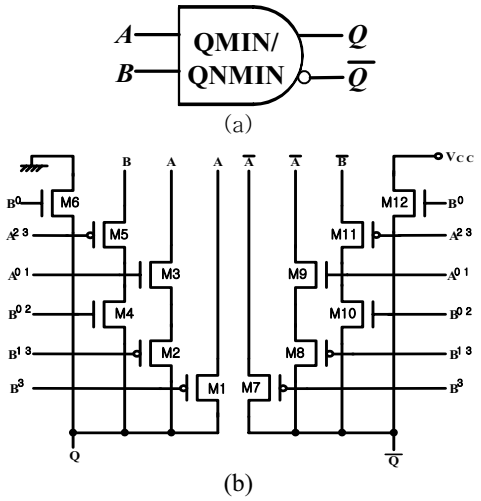


Fig. 5. (a)Symbol of the QMIN/QNMIN. (b)A circuit of the QMIN/QNMIN.

For example, when input A is 2 and B is 3, M3, M9 are turned off and M5, M11 are turned on by input A, and M4, M10, M6, M12 turned off and M1, M7, M2, M8 turned on by input B, therefore, the output is "Q=2, $\overline{Q}$=1"

Similarly, QMAX/QNMAX operation is shown as Eq.(7). The operator $\vee$ or $\oplus$ is QMAX operation.

$$x_1 \vee x_2 \vee \cdots \vee x_n = QMAX(x_1, \cdots, x_n)$$
$$x_1 \oplus x_2 \oplus \cdots \oplus x_n = QMAX(x_1, \cdots, x_n) \quad (6)$$

A QMAX function shown in Table 4 is represented to Eq.(7).

Table 4. QMAX function

B \ A	0	1	2	3
0	0	1	2	3
1	1	1	2	3
2	2	2	2	3
3	3	3	3	3

According to Eq.(7), (8) QMAX and QNMAX can be easily configured using DPL with νMOS threshold gate.

$$Y = 3 < B^3 > + A < A^{23}, B^{02} > + B < A^{01}, B^{13} > + A < B^0 > \quad (7)$$

$$Y = 0 < B^3 > + \overline{A} < A^{23}, B^{02} > + \overline{B} < A^{01}, B^{13} > + \overline{A} < B^0 > \quad (8)$$

In Fig.6(b), the operation of QMAX/QNMAX same as the operation of the QMIN/QNMIN.

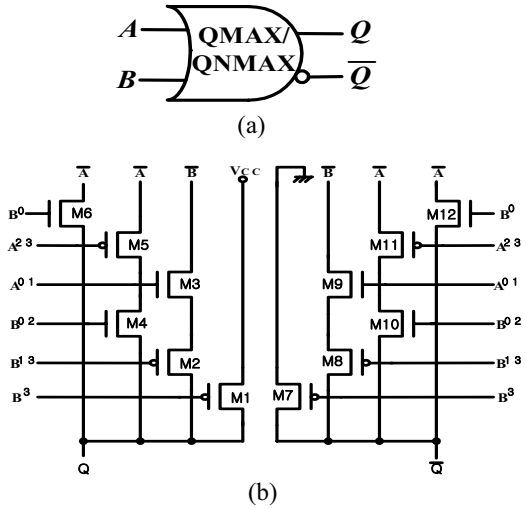


Fig. 6. (a)Symbol of the QMAX/QNMAX. (b)A circuit of the QMAX/QNMAX

B. QTS and QTD

We proposed the QTS and QTD circuit. The QTS operation is shown as Eq.(9). The QTS operator, denoted by the symbol $\boxplus$, is defined as

$$a \boxplus b = MIN(a + b, 3) \quad (9)$$

(Where $a + b$ denotes the conventional algebraic addition).
Subcases is the QTS by one, shift up, defined as

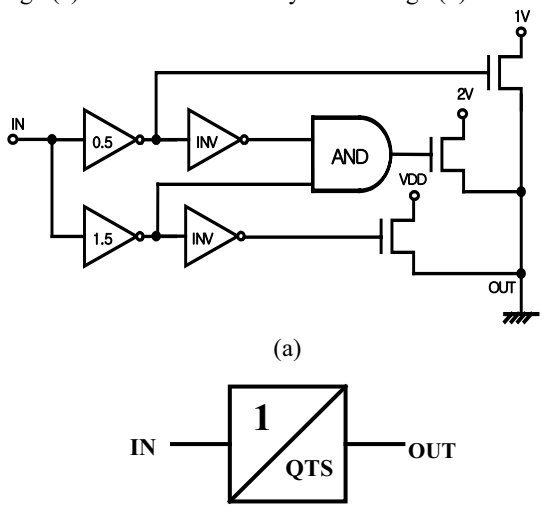
$$a \boxplus 1 = MIN(a + 1, 3)$$

A QTS function shown in Table 5 is represented to Eq.(9).

Table 5. The truth table of QTS

IN	OUT
0	1
1	2
2	3
3	3

According to Eq.(9), QTS circuit can designed like Fig.7(a) and can shown the symbol in Fig.7(b).



(a)

(b)

Fig.7. (a)Circuit of the QTS (b)Symbol of the QTS

The QTD operation is shown as Eq.(10). The QTD operator, denoted by the symbol $\boxminus$, is defined as

$$a \boxminus b = MAX(a - b, 0) \qquad (10)$$

(Where $a + b$ denotes the conventional algebraic addition).
Subcases is the QTD by one, shift up, defined as

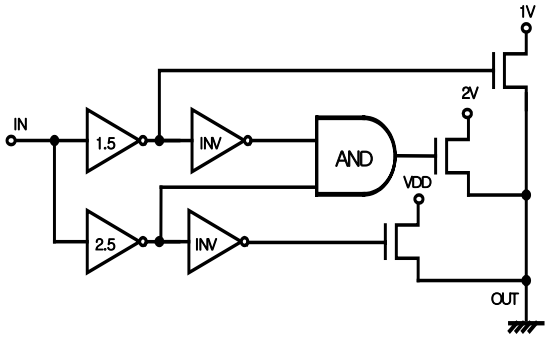
$$a \boxminus 1 = MAX(a - 1, 0)$$

A QTD function shown in Table 6 is represented to Eq.(10).

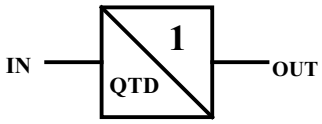
Table 6. The truth table of QTD

IN	OUT
0	0
1	0
2	1
3	2

According to Eq.(10), QTD circuit can designed like Fig.8(a) and can shown the symbol in Fig.8(b).



(a)

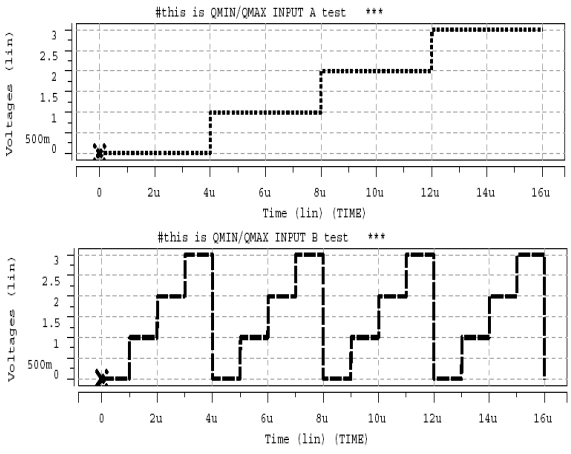


(b)

Fig.8. (a)Circuit of the QTD (b)Symbol of the QTD

IV. SIMULATION RESULTS

The HSPICE simulation of QMIN/QNMAX and QMAX/QNMAX are shown in Fig. 9(b) and 9(c), respectively.



(a)

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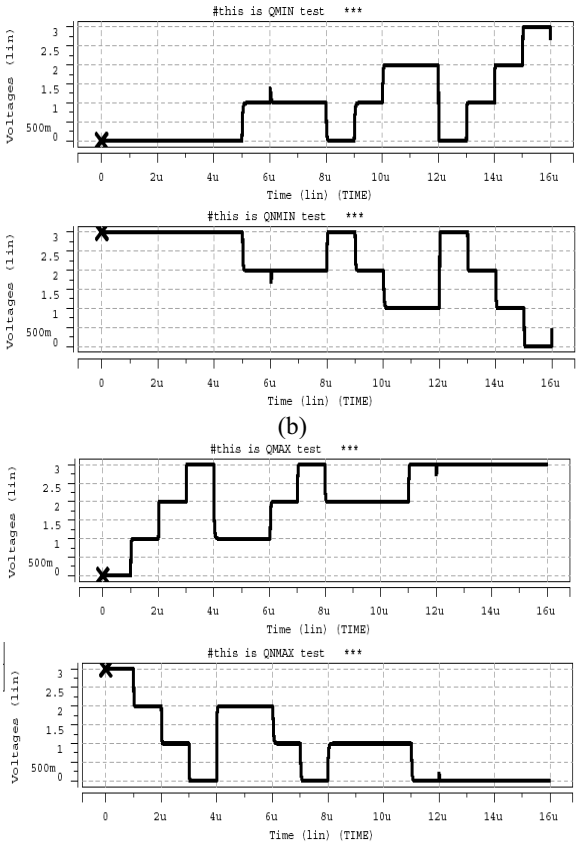


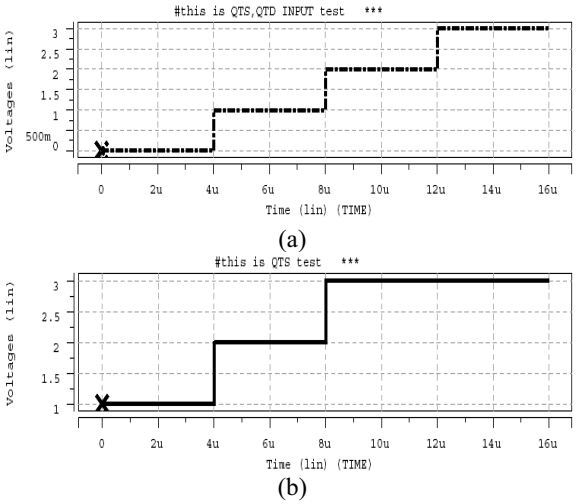
(b)

(c)

Fig.9. (a)Input of QMIN/QNMIN, QMAX/QNMAX (b)Simulation results of the QMIN/QNMIN (c)Simulation results of the QMAX/QNMAX

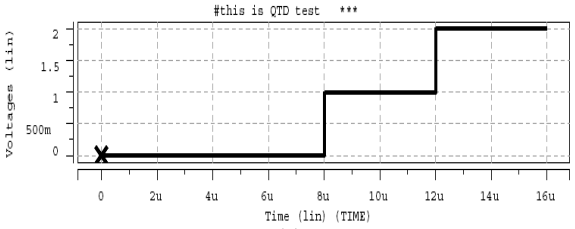
The power dissipation, QMIN/QNMIN and QMAX/ QNMAX have 4.898uW. Each component is designed at the sampling speed of 0.25MHz.

And the HSPICE simulation of QTS and QTD are shown in Fig. 10(b) and 10(c), respectively.



(a)

(b)



(c)

Fig.10. (a)Input of QTS and QTD (b)Simulation results of the QTS (c)Simulation results of the QTD

V. CONCLUSION

In this paper, we designed the quaternary logic gates such as QMIN/QNMIN and QMAX/QNMAX using DPL with νMOS threshold gate and DPL. And also we designed the QTS and QTD using DLC. The circuit verification of these logic circuits are verified by HSPICE simulation with CMOS 0.35um device parameter. Furthermore, we expect the implementation of quaternary full adder using the proposed the quaternary gates. Also we expect the quaternary ALU and past SRAM using νMOS.

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