A 200 MHz Pipelined Multiplier Using 1.5 V-Supply Multiple-Valued MOS Current-Mode Circuits with Dual-Rail Source-Coupled Logic

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Abstract— A new multiple-valued current-mode MOS integrated circuit is proposed for high-speed arithmetic systems at low supply voltage. Since a multiple-valued source-coupled logic circuit with dual-rail complementary inputs results in a small signal-voltage swing while providing a constant driving current, the switching speed of the circuit is improved at low supply voltage. As an application to arithmetic systems, a 200 MHz 54 × 54-b pipelined multiplier using the proposed circuits with a 1.5 V supply voltage is designed with a 0.8-μm standard CMOS technology. The performance of the proposed multiplier is evaluated to be about 1.4 times faster than that of a corresponding binary implementation under the normalized power dissipation. A prototype chip is also fabricated to confirm the basic operation of the multiple-valued arithmetic circuit.

I. INTRODUCTION

THE emerging trend of decreasing power dissipation in a single chip has been rapidly increased in the present deep submicron ULSI technologies. Low power dissipation can be achieved by reducing supply voltage, capacitance, and the number of active devices to perform a given function [1]–[3]. Therefore, it is important to develop a new circuit design for reducing the device counts as well as the capacitance due to the wiring complexity while providing large driving current at low supply voltage.

One possible approach to solving the above problem is to use multiple-valued logic inside a chip. Multiple-valued current-mode (MVCM) integrated circuits in particular have a potential advantage to reduce the number of active devices as well as the wiring complexity in arithmetic large-scale-integration chips because the frequently used linear sum operation can be performed simply by wiring [4]–[6]. In fact, several arithmetic integrated circuits have been designed and fabricated by MVCM logic circuits resulting in better performance compared with the corresponding binary implementation [7], [8]. However, the switching delay of a multiple-valued basic circuit becomes slower than that of a binary one because the minimum driving current of the multiple-valued basic circuit is smaller than that of the binary one. This effect is accelerated at lower supply voltage because the driving capability is proportional to the square of the supply voltage. To solve this

problem, a new multiple-valued basic circuit with high driving capability at low supply voltage must be developed for deep submicron ULSI chips.

This paper presents the design and the implementation of a new MVCM logic circuit with low supply voltage for high-speed arithmetic systems. Threshold detection is one of the most important functions in MVCM logic circuits [6]. The operating speed of any MVCM logic circuit is determined primarily by the switching delay of the threshold detector. A new threshold detector is designed by using a source-coupled logic circuit with dual-rail complementary inputs, which makes the signal-voltage swing small yet driving capability large in comparison with a conventional circuit with a single-rail input [9].

Moreover, gate-level pipelined operations are introduced for efficient utilization of the MVCM logic circuits because static power dissipation remains constant irrespective of the utilized ratio of the circuits. To realize pipelined operation, a CMOS pass gate is connected at each gate of the source-coupled transistors. Because the comparison result between a multiple-valued input and a threshold is represented by a binary voltage signal, the storage operation is easily performed using the dynamic binary storage scheme.

As a typical application to large-scale arithmetic systems, a high-speed signed-digit (SD) arithmetic pipelined multiplier is designed and fabricated by using the latched threshold detector. A basic building block of the pipelined multiplier is a latched signed-digit full adder (L-SDFA) whose operating speed is primarily determined by the switching delay of the latched threshold detector. Since the operating speed of a long-word multiplier is determined by the delay of an adder tree, the proposed L-SDFA is useful for high-speed multiplication in a pipelined manner.

In fact, it is demonstrated that under normalized power dissipation, the maximum operating speed of the proposed L-SDFA is 1.4 times faster than that of a binary CMOS implementation with a 1.5 V supply voltage. On the basis of the L-SDFA, a 54× 54-b multiple-valued pipelined multiplier is designed. As a result, the maximum operating frequency of the multiplier is evaluated to be about 200 MHz. Moreover, prototype CMOS integrated circuits for the pipelined multiplier have been fabricated using a 0.8-μm standard CMOS technology, and their basic operations have been confirmed.
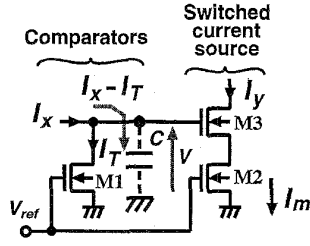
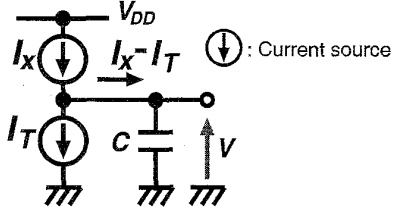Fig. 1. Threshold detector with a single-rail input.

Fig. 2. Equivalent circuit of the comparator.

II. PRINCIPLE OF A HIGH-SPEED MVCM LOGIC CIRCUIT

In MVCM logic circuits, threshold detection is one of the most important functions. It is well-known that the operating speed of any MVCM logic circuits is primarily limited by the delay of the threshold detectors. In the following section, we discuss how to improve the switching speed of the threshold detector at a low supply voltage.

### A. Delay of a Threshold Detector with a Single-Rail Input

The function of a threshold detector is to detect an input current level and to regenerate the multiple-valued current. The conventional threshold detector consists of a comparator and a switched current source as shown in Fig. 1. If the input current I_x is less than the threshold current I_T, the output voltage V of the comparator is low. This means that the switched current source is off, and the output current I_y remains zero. On the other hand, if I_x is greater than I_T, V becomes high, and the switched current source turns on. Then, the output current I_y becomes I_m. Consequently, the function of the threshold detector is defined as follows:

$$I_y = \begin{cases} 0 & \text{if } I_x < I_T \\ I_m & \text{if } I_x \geq I_T \end{cases}. \tag{1}$$

Assuming that the enhancement-mode NMOS transistor M1 operates in the saturation region with sufficient reference voltage V_{ref}, the equivalent circuit of the comparator is obtained as shown in Fig. 2. The delay of the threshold detector is determined by the charge (or discharge) time for the load capacitance C as follows:

$$t_{TD} \propto C \frac{V_{DD}}{|I_x - I_T|} \tag{2}$$

where t_{TD} and V_{DD} are the maximum delay and the supply voltage of the comparator, respectively. The load capacitance C is given by the sum of the gate capacitance of M3 and the parasitic capacitance of M1.
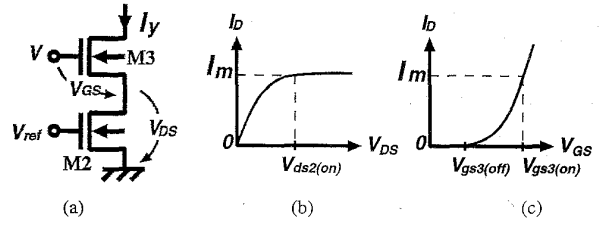
Fig. 3. Conventional switched current source. (a) Circuit diagram. (b) I_D-V_{DS} characteristic of M2. (c) I_D-V_{GS} characteristic of M3.

The delay of the threshold detector can be reduced by decreasing the supply voltage V_{DD} since the current $(I_x - I_T)$ is a constant and is independent of the supply voltage. The minimum supply voltage depends on the input voltage swing required for the switched current source.

Fig. 3 shows the conventional switched current source which consists of the NMOS transistor M2 to produce the constant current I_m and the NMOS transistor M3 to control the current. The input voltage swing ΔV_1 required for the switched current source is determined by the sum of two switching voltage swings of the transistors M2 and M3 because they are connected in series. As shown in Fig. 3, let us denote the minimum drain-to-source voltage of the transistor M2 in saturation region, the gate-to-source voltage of the transistor M3 at $I_D = I_m$, and the threshold voltage of M3 as the symbols $V_{ds2(on)}$, $V_{gs3(on)}$, and $V_{gs3(off)}$, respectively. Then, the voltages $V_{1(on)}$ and $V_{1(off)}$, at which the switched current source is turned on and off, respectively, are written as follows:

$$V_{1(on)} = V_{ds2(on)} + V_{gs3(on)} \tag{3}$$

and

$$V_{1(off)} = V_{gs3(off)}. \tag{4}$$

Using (3) and (4), the input voltage swing ΔV_1 required for the switched current source is given as

$$\begin{aligned} \Delta V_1 &= V_{1(on)} - V_{1(off)} \\ &= V_{ds2(on)} + V_{gs3(on)} - V_{gs3(off)}. \end{aligned} \tag{5}$$

As a result, the supply voltage is required to be high, which causes increased delay of the threshold detector.

B. Delay of a Threshold Detector with Dual-Rail Inputs

Fig. 4 shows the proposed threshold detector composed of two comparators and one switched current source, where $I_{x'}$, I'_T, and $I_{y'}$ are the complementary signals of the input, the threshold, and the output current, respectively. If the input current level takes R values, the three pairs of the complementary signals satisfy the following equations:

$$I_x + I_{x'} = R - 1 \tag{6}$$

$$I_T + I_{T'} = R - 1 \tag{7}$$

$$I_y + I_{y'} = I_m \tag{8}$$

where + and − indicate an arithmetic addition and a subtraction, respectively. In the following discussion, we denote a pair of the complementary currents I_x and $I_{x'}$ as $(I_x, I_{x'})$.
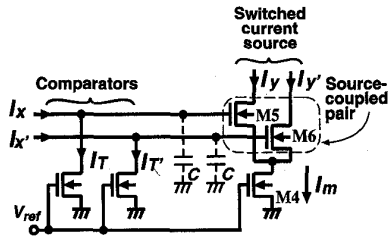
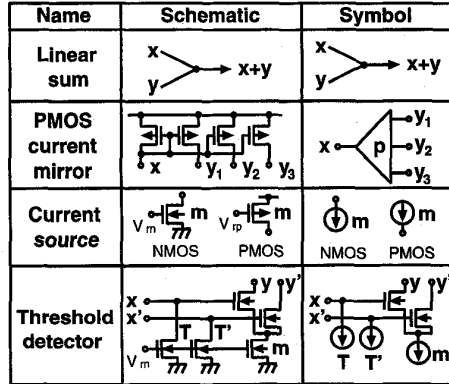Fig. 4. Threshold detector based on dual-rail source-coupled logic.

Fig. 5. Basic building blocks.

TABLE I
THREE-VALUED CURRENT LEVEL. (I_o: UNIT CURRENT)

Logic value	-1	0	1
a_i, b_i, w_i, c_i, s_i	0	I_0	$2I_0$
$a_i^t, b_i^t, w_i^t, c_i^t, s_i^t$	$2I_0$	I_0	0

TABLE II
FIVE-VALUED CURRENT LEVEL

Logic value	-2	-1	0	1	2
z_i	0	I_0	$2I_0$	$3I_0$	$4I_0$
z_i^t	$4I_0$	$3I_0$	$2I_0$	I_0	0

3) *PMOS Current Mirror:* A PMOS current mirror pro-
duces several replicas of an input current. The current
mirror also has the function of inverting the current
direction.

4) *Threshold Detector:* The function of a threshold detec-
tor is to detect an input current level and to regenerate
the multiple-valued current. The input and the output
in the proposed threshold detector based on dual-rail
source-coupled logic are represented by a pair of com-
plementary current levels.

If transistor M4 has the same dimensions with M2, and
both transistors M5 and M6 have the same dimensions with
M3, the input voltage swing can be reduced in the switched
current source based on dual-rail source-coupled logic. The
output current I_m is controlled by the source-coupled pair of
M5 and M6 with the dual-rail complementary inputs. Since
either M5 or M6 is always turned on, the current I_m is always
flowing through M4. The input voltage swing ΔV_2 to switch
the current I_m is given by

$$\Delta V_2 = V_{gs3(on)} - V_{gs3(off)}. \tag{9}$$

Equation (9) indicates that the input voltage swing for the
proposed switched current source becomes independent from
$V_{ds2(on)}$. As a result, the supply voltage V_{DD} can be reduced
for the same driving current I_m, so that the switching speed of
the proposed threshold detector becomes high at a low supply
voltage.

C. Basic Building Blocks of MVCM Logic Circuits

Fig. 5 shows the basic building blocks of the proposed
MVCM logic circuit. By the combination of the proposed
threshold detectors and the other components, we can design
high-performance MVCM logic circuits.

1) *Linear Summation:* The most attractive feature of
MVCM logic circuits is that linear summation can be
performed by wiring without active devices, so that the
resulting arithmetic circuits become quite simple.

2) *Current Source:* A current source can be designed by an
enhancement-mode NMOS (or PMOS) transistor with
the reference voltage V_{rn} (or V_{rp}). The current level is
adjusted by the transistor size.

III. DESIGN OF AN SD ADDER BASED ON DUAL-RAIL SOURCE-COUPLED LOGIC

As a typical application of MVCM logic circuits, we con-
sider a design of an SD adder.

A. Radix-2 SD Addition Algorithm

The radix-2 SD number representation using a symmetrical
digit set $\{-1, 0, 1\}$ is defined as follows [10], [11]:

$$X = (x_{n-1} \cdots x_1 x_0) = \sum_{i=0}^{n-1} x_i \cdot 2^i \tag{10}$$

where $x_i \in \{-1, 0, 1\}$. The redundancy allows totally parallel
arithmetic operations.

The addition of two numbers, $A = (a_{n-1} \cdots a_1 a_0)$
and $B = (b_{n-1} \cdots b_1 b_0)$, where $a_i, b_i \in \{-1, 0, 1\}$, is
performed by three successive steps in each digit

$$z_i = a_i + b_i \tag{11}$$

$$2c_i + w_i = z_i \tag{12}$$

$$s_i = w_i + c_{i-1} \tag{13}$$

where the linear sum $Z = (z_{n-1} \cdots z_1 z_0)$, the intermediate
sum $W = (w_{n-1} \cdots w_1 w_0)$, the carry $C = (c_{n-1} \cdots c_1 c_0)$,
and the final sum $S = (s_{n-1} \cdots s_1 s_0)$ take the values of
$z_i \in \{-2, -1, 0, 1, 2\}$, $w_i \in \{-1, 0, 1\}$, $c_i \in \{-1, 0, 1\}$
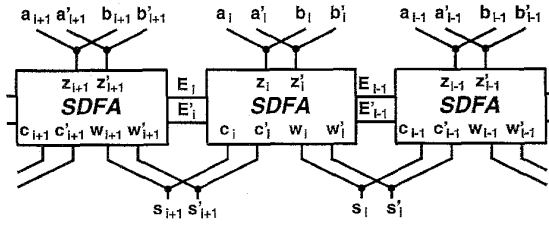and $s_i \in \{-1, 0, 1\}$, respectively.

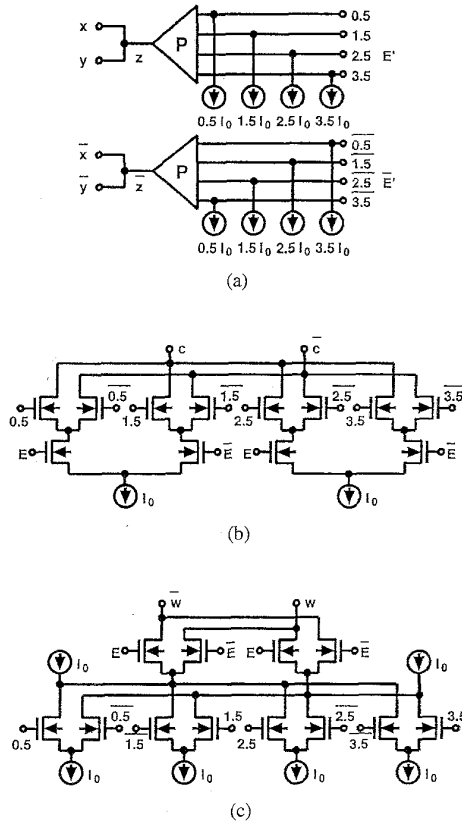Fig. 6. Radix-2 SD adder using the proposed threshold detector.

TABLE III
FOUR-VALUED THRESHOLD LEVEL

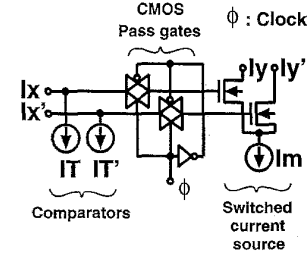| Threshold value	-0.5	-1.5	0.5	1.5
I_T	$0.5I_0$	$1.5I_0$	$2.5I_0$	$3.5I_0$
$I_{T'}$	$3.5I_0$	$2.5I_0$	$1.5I_0$	$0.5I_0$

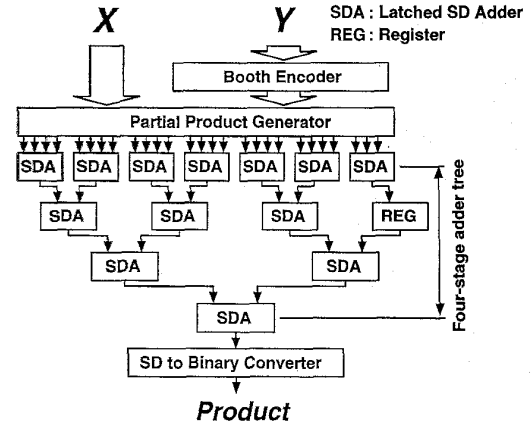Fig. 8. Latched threshold detector.

(a)

(b)

(c)

Fig. 7. Circuit diagram of the SDFA. (a) Comparators. (b) switched current sources (Carry). (c) switched current sources (intermediate sum).

To retain the final sum s_i within the set $\{-1, 0, 1\}$, c_i and w_i are determined by z_{i-1} together with z_i as follows:

$$
\begin{cases}
c_i = 1 & w_i = 0 & \text{if } z_i = 2 \\
c_i = 1 & w_i = -1 & \text{if } z_i = 1 \text{ and } z_{i-1} \geq 1 \\
c_i = 0 & w_i = 1 & \text{if } z_i = 1 \text{ and } z_{i-1} < 1 \\
c_i = 0 & w_i = 0 & \text{if } z_i = 0 \\
c_i = 0 & w_i = -1 & \text{if } z_i = -1 \text{ and } z_{i-1} \geq 1 \\
c_i = -1 & w_i = 1 & \text{if } z_i = -1 \text{ and } z_{i-1} < 1 \\
c_i = -1 & w_i = 0 & \text{if } z_i = -2
\end{cases}
\tag{14}
$$

The final sum is independent of the word length n because the carry-propagation chain is limited to one digit to the left. Therefore, the addition speed of the SD adder is higher than that of ordinary binary adders.

Fig. 9. Block diagram of the pipelined multiplier.

B. Structure of an SD Adder

In the proposed MVCM logic circuits, each digit of the SD numbers corresponds to a pair of complementary current signals. The adder inputs, the intermediate sum, the carry and final sum are represented as (a_i, a_i'), (b_i, b_i'), (w_i, w_i'), (c_i, c_i') and (s_i, s_i'), respectively, whose current levels are given in Table I. The linear sum (z_i, z_i') is also represented in Table II.

The radix-2 SD adder can be designed as shown in Fig. 6. The linear summation of (11) and (13) can be obtained by wiring without active devices. The operation of (12) is performed with an SD full adder (SDFA). The signals E_i and E_i' are used as the control ones to give the conditions of $z_{i-1} \geq 1$ and $z_{i-1} < 1$ in (14). The linear sums z_i and z_i' take five values that are transformed to decoded by four comparators set at different levels as shown in Table III. As a result, the SDFA circuit can be designed using 50 MOS transistors as shown in Fig. 7.

IV. DESIGN OF A PIPELINED MULTIPLIER

The power dissipation of the proposed circuits remains constant because current flowing in every circuit block is
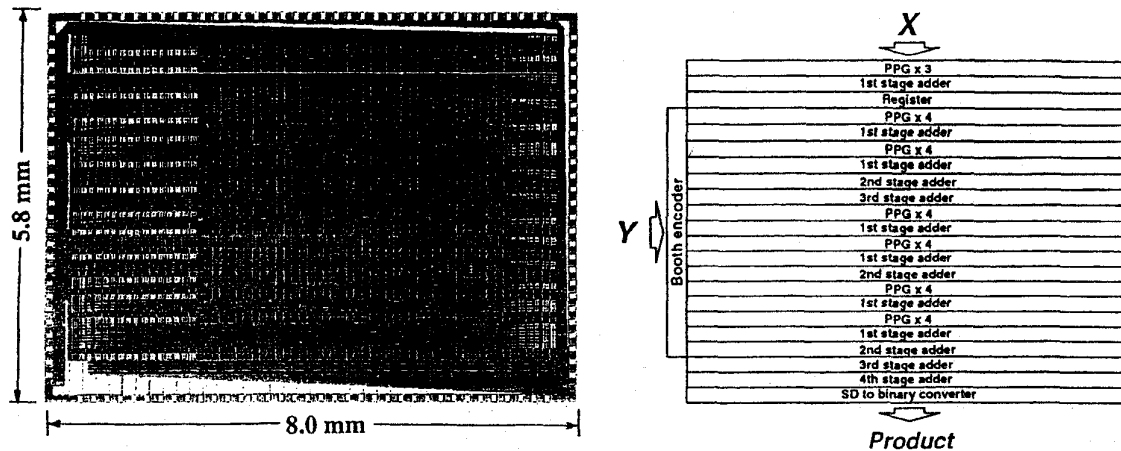
Fig. 10. Layout of the pipelined multiplier.

independent of the operating frequency. Therefore, the gate-level pipelined operation is effectively employed for high-speed processing under the constant static power dissipation. In this section, we consider a design of a 54×54-b pipelined multiplier as an application to larger scale arithmetic systems.

A. Latched Threshold Detector

In the proposed threshold detector, high-speed switching requires large power in current-mode logic circuits due to the average current. The gate-level pipelined operation is very suitable to increase the utilized ratio of the circuits. However, the pipelined operation requires pipelined registers that cause hardware overhead. Multiple-valued data storage circuits in particular become much larger than binary data storage circuits.

In the proposed latched threshold detector for dynamic multiple-valued logic circuits, the pipelined registers are designed by inserting two CMOS pass gates between the comparators and the switched current sources as shown in Fig. 8 because the outputs of the comparators correspond to the binary voltages. This design enhances the utilized ratio of the circuits to 100% with small hardware overhead.

B. Structure of a Pipelined Multiplier

The L-SDFA is constructed by inserting eight CMOS pass gates between the comparators and the switched current sources as shown in Fig. 7. Using the L-SDFA's, a 54×54-b multiple-valued pipelined multiplier can be designed as shown in Fig. 9. In the structure, a four-stage binary adder tree is realized based on the modified Booth's algorithm and four-input addition in the first stage of the adder tree and two-input addition in each subsequent stage.

Because the total operating speed is determined by the delay of the binary adder tree in a long-word multiplier, it is important to use the high-speed L-SDFA's. The other components such as a booth encoder, a partial product generator, and a SD-to-binary converter are basically designed by using the conventional binary CMOS implementation except for the interface circuit between the adder tree and the other
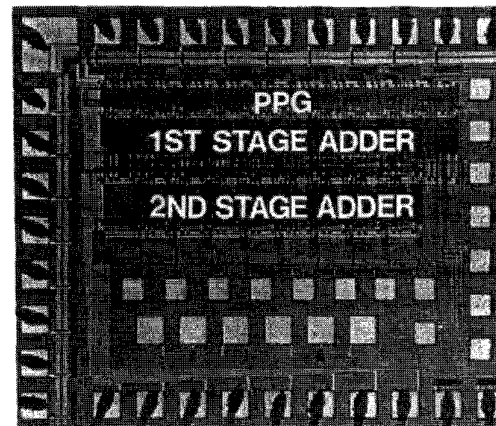

Fig. 11. Photomicrogragh of a fabricated multiplier chip.

components. Since the number of pipeline cycles for the booth encoder, the partial product generator and the SD-to-binary converter is one, one, and two, respectively, the latency of the proposed multiplier becomes eight pipeline cycles. The pipelined multiplier is performance evaluated by PSPICE simulation is shown in Fig. 10. To increase the clock frequency in the pipelined operation, the interconnections between full adder stages of adders is optimized in the layout.

V. EVALUATION

A. Implementation of Prototype Chips

To confirm the operation of the proposed MVCM logic circuit, a prototype 4×4-b pipelined multiplier chip is implemented using a 0.8-μm standard CMOS technology with double metal layers as shown in Fig. 11. The effective size of the multiplier chip is 1.7×1.4 mm^2. The typical transfer characteristics of the SDFA for the case of $-2 \leq z_i \leq 2$ are shown in Fig. 12, where a unit current level is 20 (μA). From the static transfer curves, the fluctuation of multiple threshold current levels is evaluated to be less than 5%.
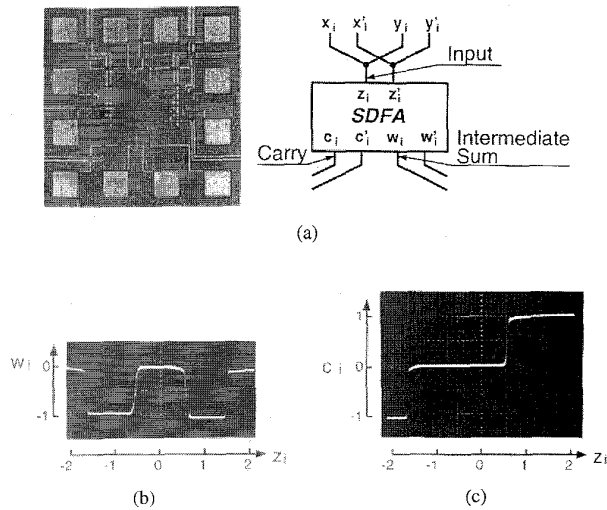
(a)

(b)   (c)

Fig. 12. Static transfer characteristic of the fabricated SDFA. (a) Chip photomicrogragh of the SDFA. (b) static transfer characteristic of the intermediate sum. (c) static transfer characteristic of the carry.
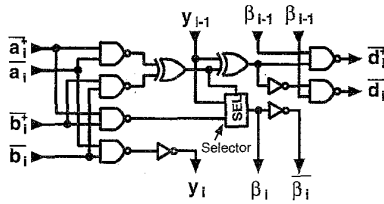

Fig. 13. Binary CMOS SDFA.

B. Comparison of Performances

Table IV summarizes the comparison of SDFA's in terms of the delay and the number of transistors under normalized power dissipation at 200 MHz. The performance is estimated by PSPICE simulation based on a 0.8-μm standard CMOS technology. Fig. 13 shows the structure of the binary CMOS SDFA that is used for the fastest multiplier [12]. In this circuit, each digit of the radix-2 SD numbers is represented by two bits. Although the switching speed of the transistors in the binary CMOS implementation is superior to that of the transistors in the multiple-valued one, the critical path of the multiple-valued implementation becomes much shorter than that of the binary CMOS one. As a result, the switching speed of the proposed SDFA is 1.3 times faster than that of the binary CMOS one at a 1.5 V supply voltage. Moreover, in spite of the complexity in the dual-rail source-coupled pairs, the transistor counts of the proposed SDFA are almost the same as that of the binary CMOS one.

Fig. 14 shows the simulated dynamic characteristic of the L-SDFA with 0.8-μm standard CMOS parameters. The maximum delay is estimated to be about 4.6 (ns). Since the pipeline cycle is determined by the worst-case switching delay of the L-SDFA, the maximum operating frequency is evaluated to be about 200 MHz. Table V summarizes the comparison of L-SDFA's. The maximum operating speed of the proposed L-SDFA is evaluated to be 1.4 times faster than that of the

TABLE IV
COMPARISON OF SDFA's

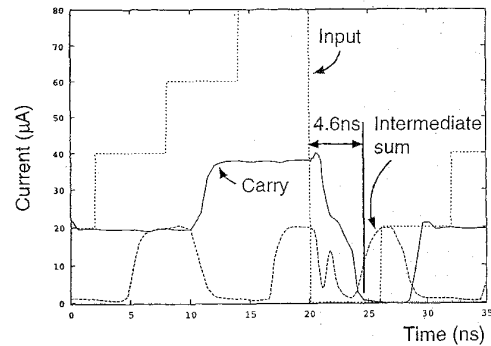| SDFA	Binary CMOS	Proposed
Supply voltage	1.5 V	1.5 V
Delay	3.9 ns	3.0 ns
Power dissipation	0.6 mW	0.6 mW
Number of transistors	48	50

PSPICE simulation based on a 0.8- μm CMOS technology

Fig. 14. Dynamic characteristic of the latched SDFA.

TABLE V
COMPARISON OF L-SDFS's

L-SDFA	Binary CMOS	Proposed
Supply voltage	1.5 V	1.5 V
Delay	7 ns	4.6 ns
Power dissipation	0.6 mW	0.6 mW
Number of transistors	52	66

PSPICE simulation based on a 0.8- μm CMOS technology

TABLE VI
FEATURES OF THE PIPELINED MULTIPLIER

Supply voltage	1.5 V
Operating frequency	200 MHz
Power dissipation	1.0 W
Chip size	5.8x8.0 mm^2

corresponding binary implementation with a 1.5 V supply voltage. Table VI shows the performance of the pipelined multiplier.

VI. CONCLUSIONS

A new threshold detector with high driving capability has been presented to improve the switching speed of the MVCM logic circuits. The use of dual-rail source-coupled logic circuits makes the input voltage swing small, so that high-speed operations can be performed at a low supply voltage. Using multiple-valued data representation and circuit technologies, the hardware overhead due to dual-rail source-coupled logic

circuits is greatly reduced. Moreover, gate-level pipelined architecture using the proposed latched threshold detectors enhances the utilized ratio of every circuit block with small hardware overhead. A prototype CMOS integrated circuit for examining the principle operation has been implemented, and we have shown that the proposed MVCM multiplier can be realized by a standard CMOS technology. As a typical application to large-scale arithmetic systems, we have designed and evaluated a high-performance 54 × 54-b multiple-valued pipelined multiplier operated at 200 MHz with a 1.5 V supply voltage.

As a future problem, it is also important to save the static power dissipation of the MVCM logic circuits in a nonpipelined operation. One approach is to make the current sources turned off when the circuit block is not effectively operated. In the proposed source-coupled logic circuit, the static power dissipation can be easily decreased by controlling the gate voltages of the current sources without inserting additional transistors. If the problem is successfully solved, we may well see an ultra-low-power multiple-valued VLSI chip for high-speed arithmetic operations.

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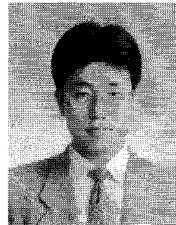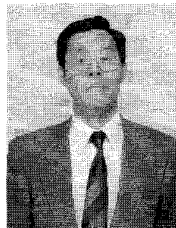
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