Multiple-Valued Signed-Digit Adder Using Negative Differential-Resistance Devices

Alejandro F. González, *Student Member*, *IEEE*, and Pinaki Mazumder, *Senior Member*, *IEEE*

Abstract—This paper describes a new signed-digit full adder (SDFA) circuit consisting of resonant-tunneling diodes (RTDs) and metal-oxide semiconductor field effect transistors (MOSFETs). The design is primarily based on a multiple-valued logic literal circuit that utilizes the folded-back I-V (also known as negative differential-resistance, NDR) characteristics of RTDs to compactly implement its gated transfer function. MOS transistors are configured in *current-mode* logic, where addition of two or more digits is achieved by superimposing the signals of individual wires being physically connected at the summing nodes. The proposed SDFA design uses redundant arithmetic representation and, therefore, the circuit can perform addition of two arbitrary size binary numbers in constant time without the need for either carry propagation or carry look-ahead. The SDFA cell design has been verified through simulation by an augmented SPICE simulator that includes new homotopy-based convergence routines to tackle the nonlinear device characteristics of quantum devices. From the simulation result, the SDFA cell has been found to perform addition operation in 3.5 nanoseconds, which is somewhat superior to other multivalued redundant arithmetic circuits reported in the literature. The SDFA cell requires only 13 MOS transistors and one RTD, as opposed to the state-of-the-art CMOS redundant binary adder requiring 56 transistors, and to the conventional multivalued current-mode adder consisting of 34 MOS transistors. In order to verify the simulation result, a prototype SDFA cell has been fabricated using MOSIS 2-micron CMOS process and GaAs-based RTDs connected externally to the MOSFET circuit.

Index Terms—Signed-digit arithmetic, multiple-valued logic, quantum electronic resonant-tunneling circuits.xxx

1 Introduction

In a conventional ripple-carry adder, the input carry bit may propagate through the bank of full adders, spanning from the least significant digit to the most significant digit. Therefore, the worst-case propagation delay in a ripple-carry adder is proportional to n, the size of the adder. Other approaches, such as carry look-ahead, can reduce the propagation delay to log n time at the expense of additional circuits that not only introduce irregularity in chip layout but also render the adder circuit less amenable to comprehensive testing. The signed-digit number system, originally proposed in 1961 by Avizienis [1], can be used in adder circuits to restrict carry propagations only to adjoining cells by eliminating the dependency of the carry output function on the carry input signal. To restrict carry propagation, signed-digit number systems employ redundant representation, in which a number different from zero can be expressed in more than one unique way. In signed-digit adders, it is possible to perform addition of two arbitrary size numbers in constant time, and redundant algorithms can, therefore, help to significantly improve the performance of arithmetic circuits in applications with large operand sizes. Signed-digit systems have been adopted by many researchers and designers in the development of high-performance arithmetic circuits [2], [3], [4], [5], but compact and efficient implementation of the signed-digit adders still remains somewhat elusive with the conventional device technologies.

As MOS technology is rapidly advancing to its physical limits of feature size shrinking, it is of paramount importance that device engineers discover alternative enabling technologies that may employ radically different device transportation phenomena, such as quantum tunneling through multiple barrier structures, single-electron-controlled charge transfer over the coulombian blockade, charge transfer over complex molecular structures, and DNA computing. Among a host of nascent technologies that seem to be extremely promising, quantum electronic resonant-tunneling devices, such as resonant-tunneling diodes (RTDs) [6], resonant-tunneling hot electron transistors (RHETs) [7], resonant-tunneling bipolar transistors (RTBTs) [8], bound-state resonant-tunneling transistors (BSRTTs) [9], etc., are the most mature and appear to be imminently viable for commercial introduction. These devices can operate at room temperature and they are compatible with conventional technologies such as heterojunction bipolar transistors (HBTs) [10], [11], and high-electron mobility transistors (HEMTs) [12], [13].

The nonlinear tunneling characteristics of these devices can be efficiently harnessed to design multiple-valued circuits requiring fewer active devices and less amount of connecting wires between them. Interconnects will predominantly govern the circuit speed in future gargantuan multibillion transistor monolithic integrated chips. Multiple-valued logic (MVL) can alleviate the interconnect delay and routing complexities since multivalued signals convey more information than binary signals, thus requiring less amount of interconnects to transmit similar bandwidth of information [14], [15]. In a signed-digit arithmetic system, multivalued signal levels are used to perform the arithmetic

• *The authors are with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109. E-mail: mazum@eecs.umich.edu.*

Manuscript received 9 June 1997; revised 25 Nov. 1997.
For information on obtaining reprints of this article, please send e-mail to: tc@computer.org, and reference IEEECS Log Number 105233.

functions much more compactly than the conventional binary arithmetic system. Resonant-tunneling devices are inherently bistable devices capable of retaining the output states after the input signals change their values. This property enables the circuit designers to develop deeply pipelined (what is termed as nanopipelining) circuits where each gate behaves as a bistable latch. This novel feature allows the circuits to obtain much higher speed and throughput. In addition to nanopipelining capability, resonant-tunneling devices can be stacked together vertically to develop multistate memories and multivalued logic gates [14], [16], [17], [18], [19].

This paper presents a multiple-valued signed-digit full adder consisting of resonant-tunneling diodes (RTDs) and MOS transistors. The proposed circuit is built compactly using only 13 MOS transistors and one two-peak RTD, in comparison to 56 transistors required by Makino et al.'s well-known CMOS redundant binary adder [3], and to 34 devices required by an efficient multivalued current-mode MOS adder proposed by Kawahito et al. [20]. The signed-digit adder in this paper implements a radix-2 arithmetic system that uses ternary digit set {–1, 0, +1}. In order to obtain a good noise performance, a three-valued logic system is used. A mockup prototype of the adder circuit was fabricated using MOSIS 2-micron CMOS process technology and the RTDs were externally added, since siliconized RTDs are not yet ready for cointegration with the standard CMOS technologies. The circuit has been tested to verify its functionality and its measured output waveforms were matched with its simulated output responses.

At present, RTDs and other quantum tunneling devices are primarily based on compound-semiconductors such as gallium arsenide (GaAs) and indium phosphide (InP). Currently, RTDs cannot be integrated with MOS devices, but vigorous efforts are being made to monolithically integrate RTDs and silicon MOS transistors. One of the approaches being pursued consists of developing NDR devices made of silicon germanium (SiGe), which is compatible with silicon technology [21], [22]. Another approach [23] involves lifting off RTDs from GaAs wafer and then bonding them onto a silicon host substrate.

The rest of this paper is organized as follows. Section 2 describes the principle of operation of the proposed signed-digit adder design. Section 3 then analyzes the MOS/RTD-based multivalued literal circuit, which is the centerpiece of the proposed signed-digit adder. In Section 4, simulation and experimental results are presented. Conclusions are made in Section 5, giving a comparison of the proposed adder design along with some other fast adder circuits.

2 Signed-Digit Full Adder Circuit Design

This section describes the operation of the proposed signed-digit full adder (SDFA) circuit. First, the required transfer characteristics for a three-valued arithmetic (radix-2) will be described. The circuit implementation of the identified transfer functions will then be presented. It was found that RTDs, in conjunction with CMOS devices, offer important benefits in terms of circuit compactness in two ways. First, CMOS devices are very useful in a current-mode logic with wired-summation of digits that saves circuit area. Second, the folded I-V characteristic of the RTD can be utilized to build high functionality literal gates which can be put together to form multiple-valued logic adders, enabling the ensuing RTD-based adder design to be even more compact.

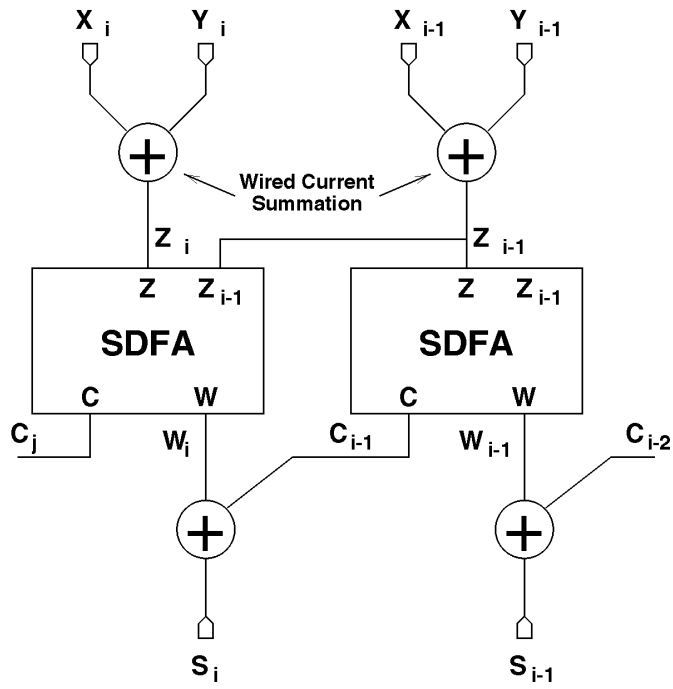


Fig. 1. Block digram of the implemented totally-parallel addition approach.

2.1 Transfer Characteristics

Fig. 1 depicts a block diagram of the signed-digit addition approach proposed in this work. Lines x_i, y_i, c_i, w_i, and s_i are three-valued, current-mode signals. Addition of x_i and y_i is achieved by simple wired-summation of currents. The function of the SDFA block is to convert the summation of input signal, z, to a two-digit representation of the sum given by digits c and w, that is, $rc + w = z$ where $r = 2$. The final sum output, s_i, is obtained by current-addition of the interim sum output, w_i, and the incoming carry signal, c_{i-1}. This addition approach corresponds to the signed-digit addition proposed by Avizienis in [1]. According to signed-digit arithmetic theory, the radix value should meet the condition $r > 2$. In this case, $r = 2$, however, which leads to the implementation of a *modified signed-digit* arithmetic [1]. An important characteristic of the modified signed-digit arithmetic is that the SDFA block requires as inputs both its corresponding input signal, z, and the input to the next less-significant adder slice, z_{i-1}. The use of input z_{i-1} in the SDFA cell is explained next.

The transfer functions of the SDFA block are defined so that w and c always represent the arithmetic value of $x + y$. Fig. 2 shows the transfer functions for the interim sum, w, and the carry, c, signals in the SDFA cell. All the digits in the graph are positive because the circuit will use only positive currents. In this case, the signed-digit 0 is represented by a current level "3," digit –2 is represented by current "1," and so on. There are two pairs of transfer functions, and the

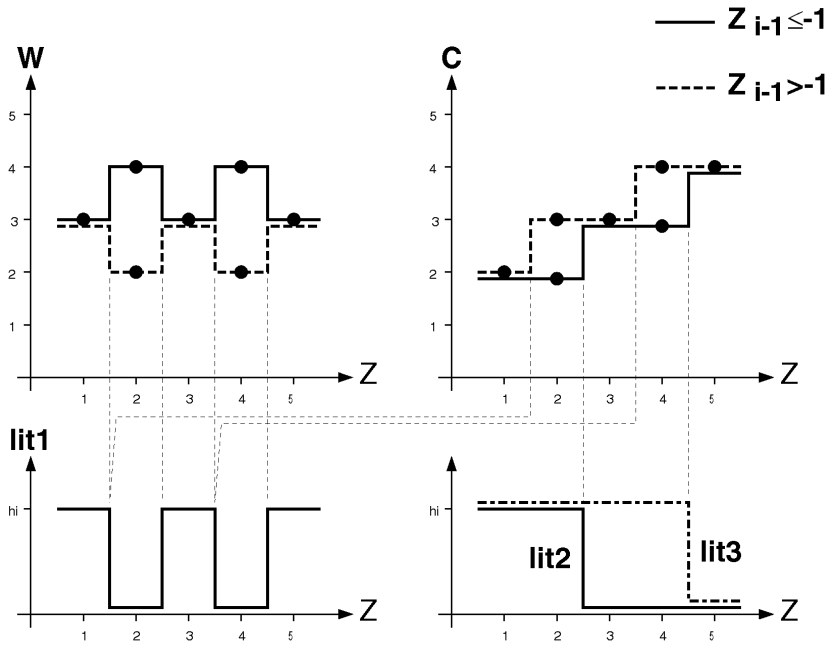


Fig. 2. Transfer function of the SDFA block.

working pair is selected by the value of z_{i-1}. This input signal is used to determine if $c_{i-1} \neq -1$, which indicates when the SDFA cell is allowed to generate an output $w = -1$ without causing invalid s current levels to be produced. If the input z_{i-1} to the previous digit was not considered, then it would be possible to generate $w = -1$ or $w = 1$ when $c_{i-1} = -1$ or $c_{i-1} = 1$, respectively. In these cases, the final sum result would be $s = -2$ or $s = 2$, which are invalid outputs for the selected radix.

Careful observation of the SDFA transfer characteristics shows that three multiple-valued literal signals can be used to describe the adder function. As seen in Fig. 2, literals *lit*1, *lit*2, and *lit*3 contain all the switching information required to define output functions w and c. This observation forms the basis of the proposed SDFA cell design, whose block diagram is depicted in Fig. 3. The input to the system is the wired summation current signal i_z. The three required literal signals are then generated in different blocks of the circuit. The literal signals are used to control switched current sources, which, in turn, synthesize the SDFA transfer functions in the *current output generator* block. Please note that the output block uses input signal $V_{\alpha_{i-1}}$ to determine which of the two sets of transfer characteristics should be used. $V_{\alpha_{i-1}}$ indicates if $z_{i-1} < -1$ and, to our advantage, its behavior is identical to literal *lit*2.

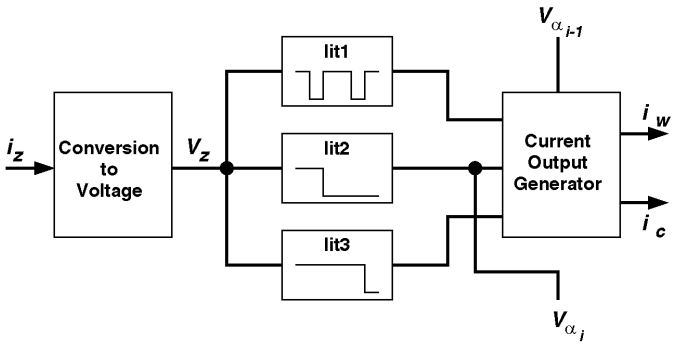


Fig. 3. Block diagram of the proposed SDFA cell.

2.2 Literal Circuit Implementation

Let us begin the description of the SDFA circuit by discussing the implementation of signal *lit*1 using RTDs. Fig. 4 shows the basic circuit used for generating the literal signals. As seen in the figure, the circuit consists of a serial connection of a resistor R_s and an RTD, where the RTD performs as a load element. The input to the circuit is the voltage V_z, which represents the wired summation $z = x + y$. In the case of *lit*1, two RTDs are used in series to obtain an equivalent two-peak characteristics. The CMOS inverter is used to sense the voltage at the node connecting the RTD and the resistor (V_{node}). The proposed literal circuit is similar to the one presented in [14]; however, the proposed design uses a complete CMOS inverter instead of a passive-load inverter.

The behavior of the voltage V_{node} is described using the load-line method (depicted in Figs. 5a and 5b). The I-V characteristics of the RTD and the resistor are plotted as the current I that flows through them with respect to the voltage V_{node}. The value of the current I is found at the point of intersection of the I-V curves. The operating point of the circuit changes as the input voltage V_z is increased because the I-V curve of the RTD is moved to the right as V_z increases. There are points where the current I suddenly decreases with increasing V_z due to the folded I-V characteristics of RTDs. Fig. 5b, shows a low-current operating point occurring after a transition from a high-current point (shown in Fig. 5a). Since the voltage V_{node} is proportional to the current I, the transitions in I are directly reflected in V_{node}. Fig. 5c displays the ideal behavior of V_{node} obtained using the load-line method.

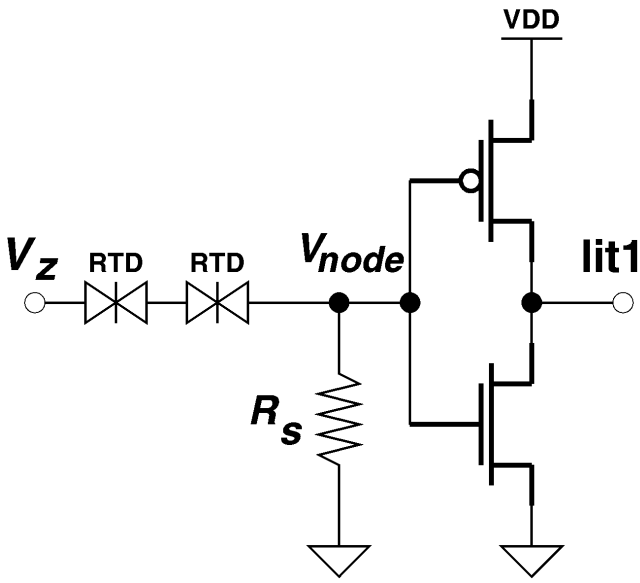


Fig. 4. Compact literal circuit using RTD and CMOS devices.

The CMOS inverter is used to sense V_{node} and, then, generate the transfer characteristic of *lit*1 using the threshold of the gate (see Fig. 5c). The CMOS inverter can be thought of as a buffer/quantizer of the RTD-resistor voltage characteristics. The CMOS gate offers a very important advantage to the literal circuit: a high input resistance that prevents the alteration of the RTD characteristics caused by draining DC currents from the node V_{node}. Fig. 5c depicts the formation of the literal signal *lit*1 by sensing V_{node}. Observe that the values of V_z where the negative transition points of literal *lit*1 take place depend on the value of the threshold voltage of the inverter (V_T).

As seen in Fig. 2, literals *lit*2 and *lit*3 are simpler than literal *lit*1. Consequently, implementing them is easier than implementing *lit*1 and no RTDs are required. Functions *lit*2 and *lit*3 correspond to threshold detectors whose threshold levels should match the switching points of the carry output function, *c*, for $z_{i-1} \leq -1$. Fig. 7 shows the implementation of literals *lit*2 and *lit*3 by means of two resistors connected in series. The ratio between the values of the two resistors for each literal determines the corresponding switching threshold levels.

2.3 Output Current Circuits

The generation of the SDFA transfer functions by means of literal signals *lit*1, *lit*2, *lit*3 is now discussed. The behavior of the literals was conceived with the purpose of achieving a simple implementation of the current output block. The approach consists of using the four controlling signals (three literals and $V_{\alpha_{i-1}}$) to activate switched current sources. These current sources are implemented with MOS devices. Fig. 6 shows the current output generator circuits. Implementing output *w* requires only three MOS transistors and two control input signals (see Fig. 6a). The interim sum circuit owes its simplicity to the similarity between the forms of function *w* and literal *lit*1. Transistor *m*1 injects a current equivalent to one logic level when *lit*1 is high. These states correspond to $z = 1, 3, 5$ in the transfer function

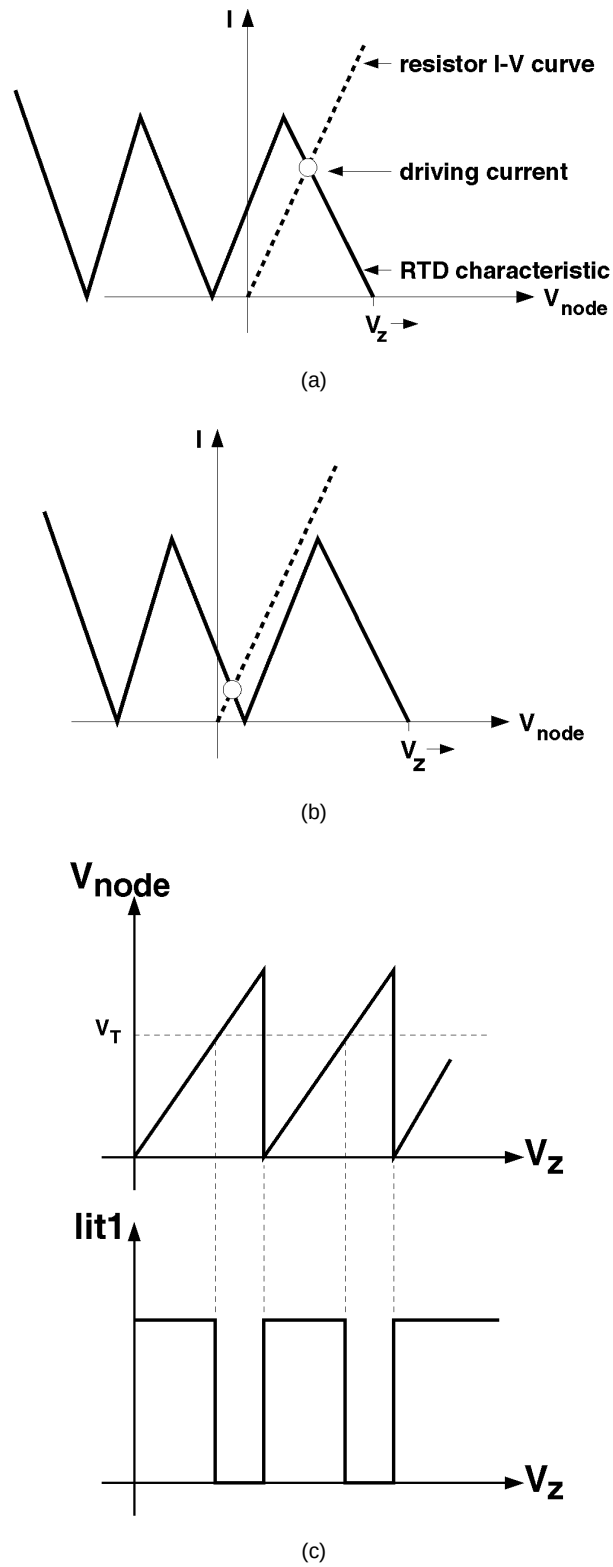


Fig. 5. (a), (b) Application of the load-line method in describing the behavior of voltage V_{node}. (c) Ideal representation of the use of the CMOS inverter in the formation of *lit*1.

shown in Fig. 2. The operating points for $z = 2, 4$ are handled by transistors *m*2 and *m*3, which inject a current equivalent to two logic levels or no current at all, depending upon the value of $V_{\alpha_{i-1}}$.

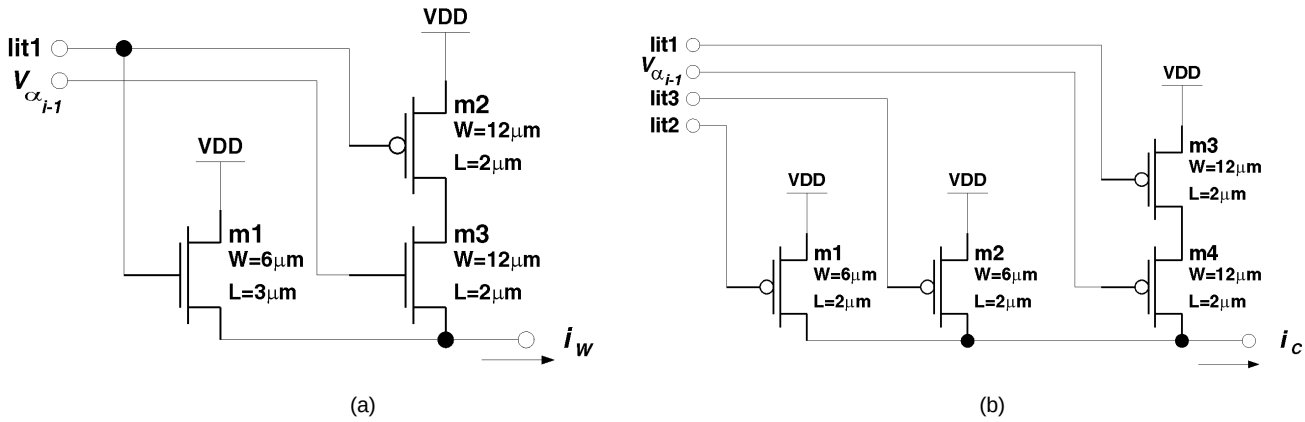


Fig. 6. Circuits for generating the (a) interim sum and the (b) carry output functions.

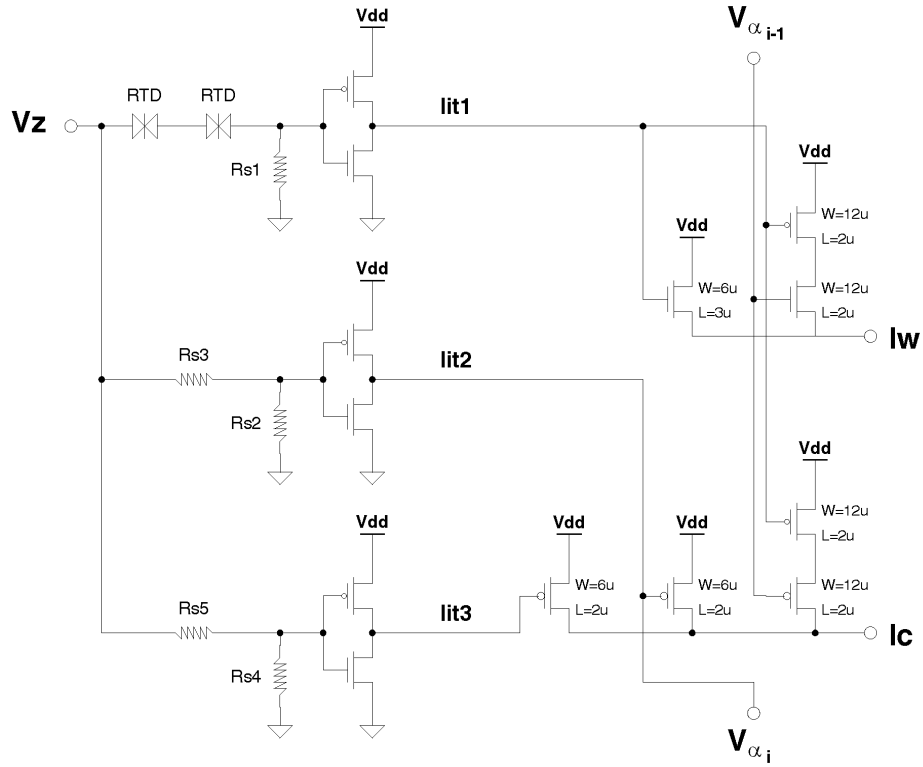


Fig. 7. Complete SDFA cell circuit.

The circuit for implementing function c is shown in Fig. 6b. In this circuit, transistors $m1$ and $m2$ produce the basic stairway form of the carry function for the case $z_{i-1} \leq -1$ (as depicted in Fig. 2). Transistors $m3$ and $m4$ are used to generate the correct carry output current $z_{i-1} > -1$ by injecting one logic level of current at the operating points where the two cases of the output function c are different (z = 2, 4). Please note that *lit*1 controls these operating points because they coincide with the zero-level points of this literal signal. Also note that the current output functions generated by the described circuits are not identical to the ideal transfer functions shown in Fig. 2. The difference lies in the current output levels. While the ideal transfer function sweeps current levels 2, 3, and 4, the given output circuits generate signals that sweep levels 0, 1, and 2. This represents no problem at all. Since only positive current signals are used, it is always necessary to perform a shift correction after every wired-addition, and the amount of this correction is smaller if the lowest current levels possible are used. Fig. 7 shows a diagram of the SDFA circuit.

3 Transient Analysis of Multivalued Literal Circuit

In this section, we analyze the propagation delay of the RTD-based literal circuit. As expected, the propagation delay is a function of the series resistance, R_s, and the RTD characteristics. The analysis yields the best value of the resistance R_s for optimal propagation delay. A piecewise linear RTD model, shown in Fig. 8, is assumed in the analysis.

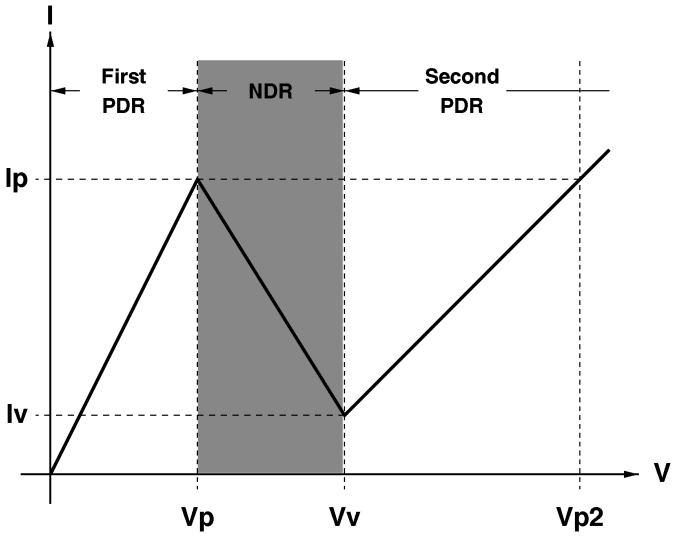


Fig. 8. Piecewise linear current-voltage RTD characteristics used in analysis.

TABLE 1
RTD PARAMETERS

Parameter	Symbol	Value
Peak Voltage	V_p	0.3 V
Peak Current	I_p	7.0 mA
Valley Voltage	V_v	0.6 V
Valley Current	I_v	0.7 mA
Second Voltage	V_{p2}	1.0 V
Peak-to-Valley Current Ratio	$PVCR = I_p/I_v$	10
Voltage Difference	$V_{pp} = V_{p2} - V_p$	0.7 V
First Positive Resistance	$R_{p1} = \frac{V_p}{I_p}$	42.9 Ω
Negative Differential Resistance	$R_n = \frac{V_v - V_p}{I_v - I_p}$	–47.6 Ω
Second Positive Resistance	$R_{p2} = \frac{V_{p2} - V_v}{I_p - I_v}$	63.5 Ω
Capacitance in PDR1 region	C_{be1}	3 fF
Capacitance in NDR region	C_{be2}	3 fF
Capacitance in PDR2 region	C_{be3}	2 fF

Observing Fig. 5b, one can see that, in order to have a sharp transition in V_{node}, $R_s < |R_n|$ where R_n is the negative differential-resistance of the RTD. From the RTD model, R_n can be written as

$$R_n = \frac{V_v - V_p}{I_v - I_p},$$

where V_p and V_v are the peak and valley voltages, respectively, and I_p and I_v are the corresponding peak and valley currents. In the given resistor-RTD topology, the maximum output voltage is given by the product of the peak current of the RTD and the value of the resistor, that is, $V_{node(max)} = I_p R_s$. On the other hand, we just saw that

$$R_s < \left| \frac{V_v - V_p}{I_v - I_p} \right|. \quad (1)$$

Therefore,

$$V_{node(max)} = I_p \frac{V_v - V_p}{I_p - I_v}.$$

Assuming a high peak-to-valley ratio ($I_p \gg I_v$), $V_{node(max)}$ can be expressed as

$$V_{node(max)} \approx V_v - V_p. \quad (2)$$

A high value of $V_{node(max)}$ is needed to switch the CMOS inverter because V_{node} has to be larger than the threshold of the inverter, V_T. Therefore, from (2), $V_v - V_p$ should be high. At the same time, from (1), $(V_v - V_p) \propto R_s$. Hence, R_s will have to be large, too, which helps to improve input resistance. However, large $V_v - V_p$ is a limiting factor for RTDs and input voltage ranges. In this particular design, the RTD characteristics were predetermined by the process and the problem consisted in selecting R_s. Table 1 describes the characteristic parameters of the RTD which were used in the analysis. In the table, *Second Voltage* is defined as the voltage $V_{p2} > V_v$ for which the current through the RTD is exactly I_p. C_{be1} through C_{be3} are intrinsic parasitic capacitances across the RTD in the three regions of operation of the device. It is important to note that the values of the current and capacitance parameters are determined by the size of the RTD.

Dynamic hysteresis is a very important factor in the selection of R_s. Dynamic hysteresis is the shifting of the RTD I-V characteristics for a dynamic input signal due to the displacement current flowing through the parasitic capacitor C_{be} [24]. The amount of shifting (hysteresis) is larger in the NDR region than in the positive differential-resistance (PDR) region because the current flowing through the RTD decreases, while the displacement current tends to increase due to a positive slew rate input. The effect of dynamic hysteresis can be expressed as a delay between the expected DC I-V characteristics and the transient response for a given positive slew rate input. The amount of this delay and its relation to the value of R_s can be calculated by performing the corresponding transient analysis of the circuit. Fig. 9 depicts the equivalent circuits for each of the operating regions of the RTD. Please note that the piecewise linear model of the RTD was used. In the diagrams, C_g is the load capacitance presented by the CMOS inverter of the literal circuit. With the exception of R_n, for which the negative sign is written explicitly in the circuit schematic, the circuit elements are assigned according to the RTD parameters presented in Table 1.

In order to find the delay at V_{node}, it is necessary to obtain the time $t_{dynamic}$ when $I_{Rs} = (I_p - I_v)/2$ in the NDR region of operation (Fig. 9c). This operating point is selected because it gives the worst case delay. The delay time t_{delay} is obtained by comparing the transient time $t_{dynamic}$ with the static time t_{static}. That is, $t_{delay} = t_{dynamic} - t_{static}$, where t_{static} is the delay for the current to reach the same operating point in the static equivalent of the circuit (without parasitic capacitances). The transient response analysis of the circuit is done in two parts. The first part is for the first PDR region of operation of the RTD, which is modeled by the circuit shown in Fig. 9b. Analyzing the first region of operation allows the calculation of the transient time when the current through the RTD reaches I_p. This information is used to obtain the initial conditions required in the second part of the analysis. The

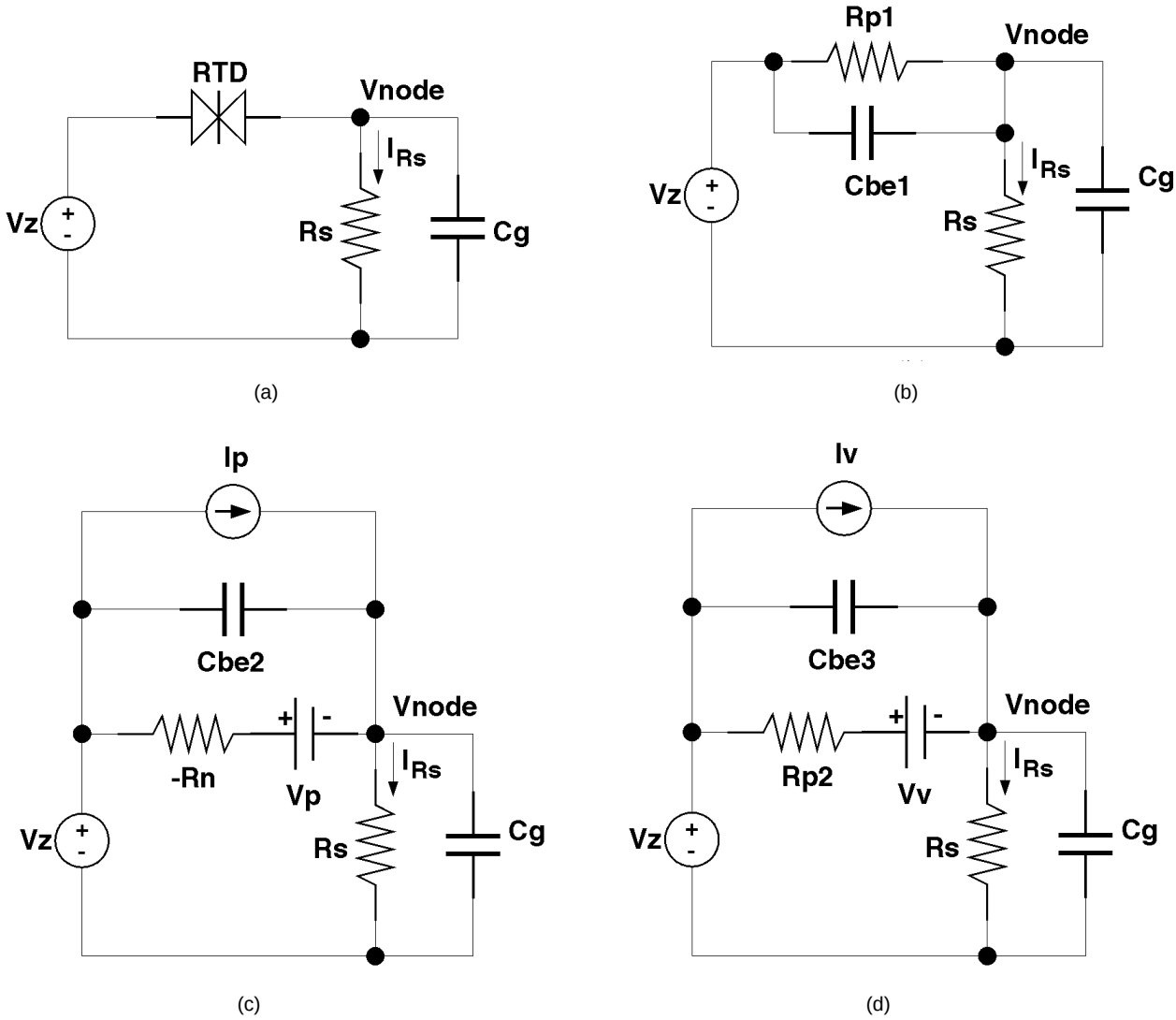


Fig. 9. Circuits used in the resistor-RTD circuit transient analysis. (a) Original circuit. Equivalent circuit in the (b) first PDR region, (c) NDR region, and (d) second PDR region.

second part is done for the NDR region of operation of the RTD, whose equivalent circuit is shown in Fig. 9c. In this part, the delay time $t_{dynamic}$, up to the operating point of interest ($I_{Rs} = (I_p + I_v)/2$), is obtained.

The first part of the analysis (PDR region) is done as follows. Please refer to Fig. 9b for this discussion. The transient response is analyzed by solving the node equations for V_{node} in time. The flow of currents at V_{node} is written as

$$\frac{V_z(t) - V_{node}(t)}{R_{p1}} + C_{be1}\frac{d}{dt}\left(V_z(t) - V_{node(t)}\right) = \frac{V_{node}(t)}{R_s} + C_g\frac{d}{dt}\left(V_{node}(t)\right). \quad (3)$$

As mentioned previously, the input signal V_z is assumed to be a ramp with slew rate S_R, that is,

$$V_z(t) = S_R t. \quad (4)$$

Solving the linear differential equation (3) with (4) and the initial condition $V_{node}(0) = 0$ yields the following expression for V_{node}:

$$V_{node}(t) = \frac{R_s S_R t}{R_{p1} + R_s} + \frac{S_R R_{p1} R_s}{R_{p1} + R_s}\left[C_p - \frac{R_s\left(C_g + C_{be1}\right)}{R_{p1} + R_s}\right]\left(1 - e^{-\alpha_1 t}\right), \quad (5)$$

where

$$\alpha_1 = \frac{R_{p1} + R_s}{R_{p1}R_s\left(C_g + C_{be1}\right)}.$$

To find the initial conditions for the second part of the analysis, (5) is used to solve

$$V_z(t_a) - V_{node}(t_a) = V_p,$$

where t_a is the time at which the RTD enters the NDR region of operation. Using t_a, the final value, V_{za}, of the input signal when the operation of the circuit leaves the PDR region ($V_{za} = S_R t_a$) is determined. V_{za} is the initial value for the input variable V_z in the second part of the analysis.

The second part of the analysis is performed in a similar fashion. In order to make things more simple, a new time reference is used. Considering this assumption and the previous result, the input variable is expressed as

$$V_z(t) = S_R t + V_{za}. \quad (6)$$

The schematic diagram in Fig. 9c depicts the equivalent circuit for the NDR region of operation. A negative sign is written for the negative differential-resistor, and the analysis is performed accordingly. This is done with the purpose of making the negative resistor more explicit. R_n in this case is the absolute value of the negative differential-resistance presented in Table 1. It is now easy to obtain the differential equation describing the operation of the circuit at V_{node}:

$$I_p + C_{be2}\frac{d}{dt}\left(V_z(t) - V_{node}(t)\right) + \frac{V_z(t) - V_{node}(t) - V_p}{-R_n} = \frac{V_{node}(t)}{R_s} + C_g\frac{d}{dt}V_{node}(t). \quad (7)$$

This equation is solved using the initial condition $V_{node}(0) = V_{za} - V_p$, which yields

$$V_{node}(t) = \frac{R_s\left(S_R t + V_{za}\right)}{R_s - R_n} + \frac{R_s}{R_n - R_s}\left[V_p + I_p R_n + S_R R_n C_{be2} + \frac{S_R R_n R_s\left(C_g + C_{be2}\right)}{R_n - R_s}\right]\left(1 - e^{\alpha_2 t}\right) - \left(\frac{R_n}{R_s - R_n}V_{za} + V_p\right)e^{-\alpha_2 t}, \quad (8)$$

where

$$\alpha_2 = \frac{R_n - R_s}{R_n R_s\left(C_g + C_{be2}\right)}.$$

Expression (8) is used to calculate the time t_b when the current through the RTD/resistor reaches the operating point of interest ($I_{R_s} = (I_p + I_v)/2$). This time is obtained by solving

$$\frac{V_{node}(t_b)}{R_s} = \frac{I_p + I_v}{2}.$$

The dynamic time is calculated as $t_{dynamic} = t_a + t_b$. To calculate t_{static}, a similar type of analysis in two steps is done. The only difference is that the calculation is for the DC transfer characteristics of the RTD, hence, the parasitic capacitors are eliminated. The delay time is calculated as the difference between dynamic and static times: $t_{delay} = t_{dynamic} - t_{static}$. Analyzing the dynamic hysteresis is useful in finding the best values for the resistor R_s. Since it is not possible to obtain a closed form solution for t_{delay}, computer tools were used to plot t_{delay} for several values of R_s. Fig. 10 shows the graph obtained for the given RTD characteristics using the method described. The experiments showed that t_b is always very small because the transient of V_{node} in the NDR region is very sharp. Therefore, the delay time is predominantly determined by the time, t_a, taken to reach $I_{R_s} = I_p$.

The criteria for selecting R_s is a trade-off between the delay and the input resistance of the literal circuit. While it is necessary to minimize the delay of the configuration, it is also necessary to maximize the input resistance. The highest value of R_s such that the delay is not sharply increased is then selected (Fig. 10). Using this criteria and the graph, $R_s \leq 35$ ohms is considered a reasonable value. Please note that the input resistance of the literal circuit is given by the sum of R_s and the positive resistance of the RTD.

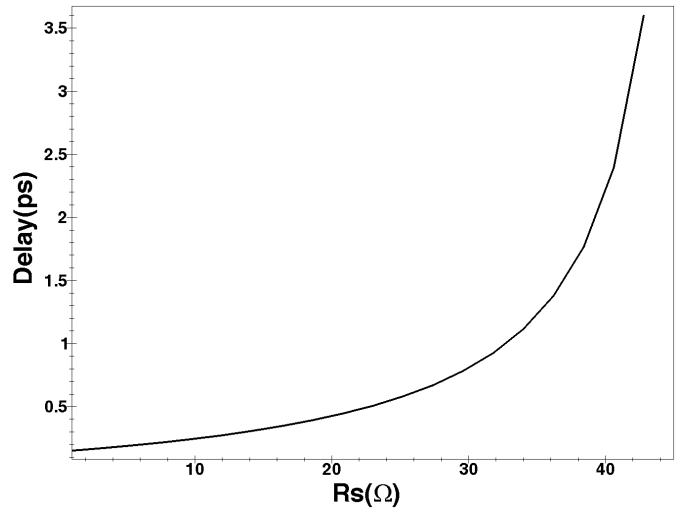


Fig. 10. RTD-based literal circuit delay with respect to R_S.

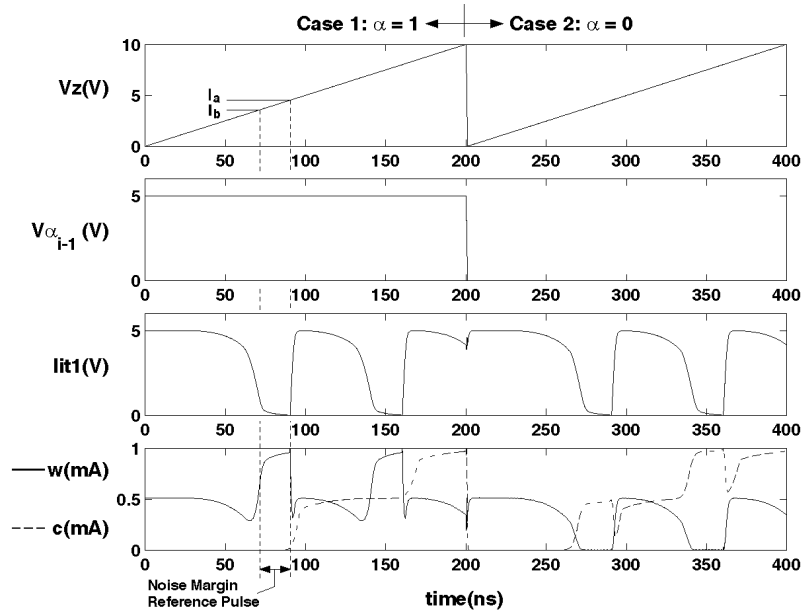
4 Results

This section describes the simulation experiments aimed at verifying and evaluating the proposed SDFA design. It also presents the prototype testing results and some of the issues related to the implementation of the prototype.

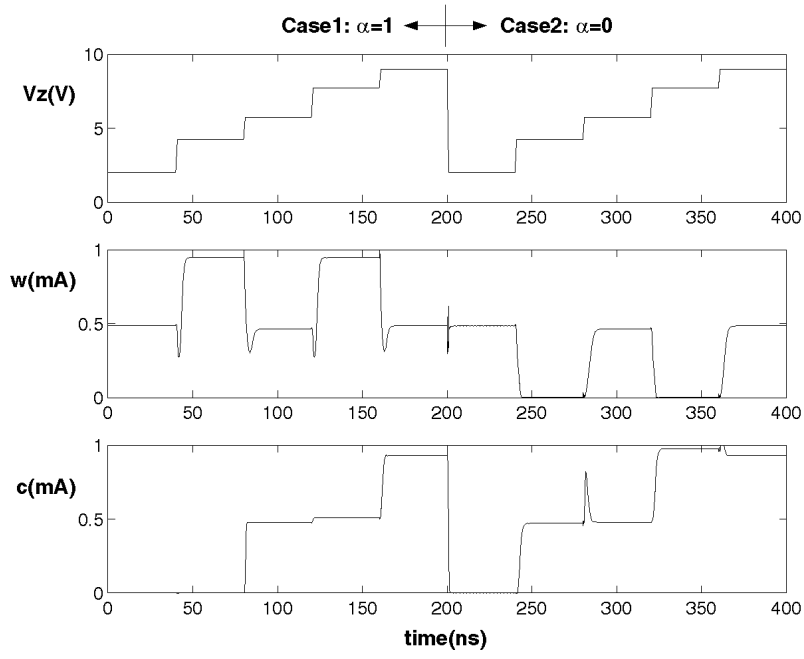
4.1 Simulation

The proposed SDFA circuit was verified using NDR-SPICE [25], [26], [27]. This circuit simulation tool includes SPICE models for RTDs and other NDR devices. The simulator also makes use of special convergence routines that eliminate false oscillations and other convergence problems that arise when simulating NDR-based circuits with conventional circuit simulators. Fig. 11a shows a transient analysis output trace obtained from a simulation of the SDFA circuit. This simulation experiment includes both cases for input $V_{\alpha_{i-1}}$: $z_{i-1} \leq -1$ and $z_{i-1} > -1$. Another important characteristic of this experiment is that the input signal is a ramp. This type of input is useful for studying the transfer characteristics of the circuit, including noise margins and identification of logic levels. Performance figures such as power consumption and speed are estimated by means of a second simulation experiment. In the second experiment, the input signal has fast transients in order to avoid contribution of the input signal rise and fall times to the delay measured at the output. In the second experiment, the input signal V_z is stepped through its different logic levels, which were determined in the first experiment. The simulation traces obtained in the second experiment are shown in Fig. 11b. These traces show a good matching of circuit operation with respect to the desired SDFA functions shown in Fig. 2.

Table 2 summarizes the results of the measurements for both simulation experiments. The noise margin was measured in the first experiment with respect to the least wide



(a)



(b)

Fig. 11. Circuit simulation traces for the (a) first and the (b) second experiments.

pulse in output signal w (as shown in Fig. 11a). The levels i_a and i_b of input signal V_z at 50 percent of each transition of the selected pulse of w are measured. The noise margin is obtained by assuming that the operating point is at the middle of the selected output pulse. Hence, the noise margin is half of the difference between the measured current values of signal V_z, that is, $NM = |i_a - i_b| / 2$. The value of power dissipation given in Table 2 was obtained in the second simulation experiment (Fig. 11b). The frequency of operation affects the value of the measured power dissipation. Finally, the delay of the circuit was measured as the time elapsed between 50 percent of the transition in the input signal, V_z, and 50 percent of the resulting transition in the output signal (in the second experiment). Both rising and falling delays were measured, but only the worst case (rising) result is given. A good characteristic of the proposed approach is that it will be able to take advantage of the progress in CMOS technology. For instance, the delay values will decrease as the circuit is implemented with more advanced CMOS processes.

4.2 Prototype Implementation

It was important to implement a working prototype in order to demonstrate the proposed principle of operation.

TABLE 2
SDFA CIRCUIT SIMULATION RESULTS

Parameter	Value
Noise Margin	0.15 mA
Power Dissipation	2.3 mW
Delay (sum)	3.5 ns
Delay (carry)	2.5 ns

With this purpose in mind, a small test circuit was designed using a standard 2-micron CMOS process. This being the initial effort in the construction of a prototype and functional testing being the main objective, the RTD and resistor elements were connected as discrete external devices to the CMOS test chip. It was necessary to make modifications on the prototype due to incompatibilities in the characteristics of the CMOS devices and the available RTDs. Based on (2) and Table 1, the highest voltage that can be produced at V_{node}, in Fig. 4, is 0.3 volt. This voltage is very low compared to the approximately 2.5-volts threshold of an inverter in the available CMOS process, where V_{DD} = 5 volts. In the future, RTD and CMOS characteristics will be brought closer together by CMOS scaling and the use of lower power supply voltages. However, given the physical limitations of MOS devices, it will also be necessary to modify the characteristics of RTDs.

For the SDFA prototype, it was necessary to modify the implementation as follows. The modification consisted of replacing the inverter of all the literal circuits by a voltage comparator, as shown in Fig. 12a. Fig. 12b shows the comparator circuit used in the SDFA prototype. This is not the most compact option for solving the problem, but it is the most flexible. Instead of altering the threshold voltage of the inverter by using circuit techniques, such as replacing the PMOS transistor of the inverter by a resistive load, the design allows for the implementation of an adjustable threshold voltage through an external reference, V_{ref}. This approach has the disadvantage of using more transistors and a reference voltage. However, it provides the important benefit of increased flexibility. Therefore, the use of a comparator is considered advantageous and appropriate for the test chip prototype. Nevertheless, mature implementations will use the simple inverter.

Another possible modification of the SDFA prototype is motivated by the need for uniformity of the devices in the current output generator module. An important difference between the interim sum and carry circuits shown in Fig. 6 lies in the types of MOS devices they use. While the carry circuit uses only one type of transistor, the interim sum uses both NMOS and PMOS devices. Using only one type of transistor gives the carry circuit two advantages. First, the switching times of the devices are more uniform. And, second, there is a better control of the current output levels because there are no different transconductance values for different types of devices. If a *w* current generator using only PMOS devices was required, it would then be necessary to insert two inverters in the SDFA circuit to generate the complements of literal signals *lit*1 and *lit*2. In the test chip, one of the SDFA cell prototypes was built using this approach. The microphotograph of the chip is shown in Fig. 13b. Fig. 13a shows a microphotograph of the simple SDFA

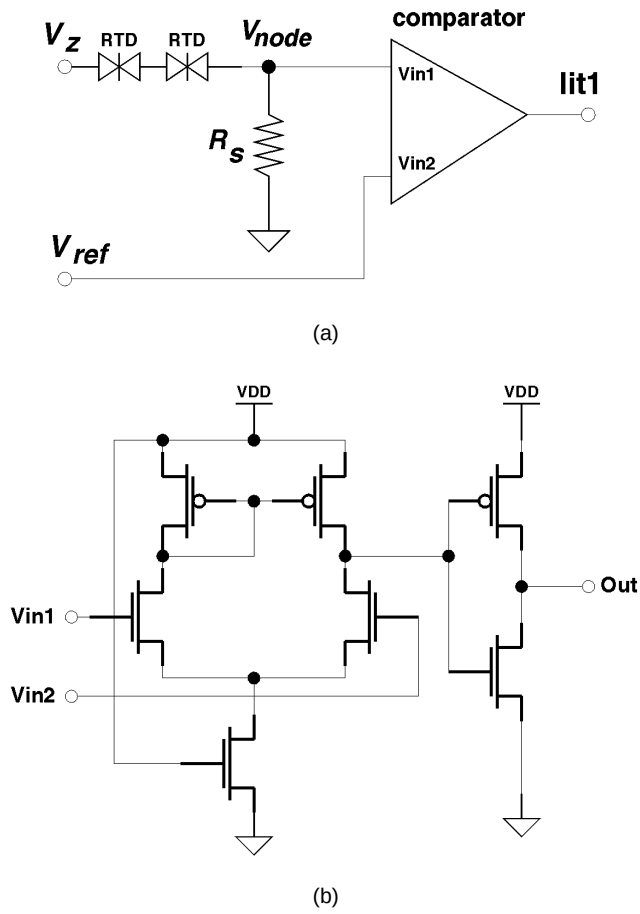


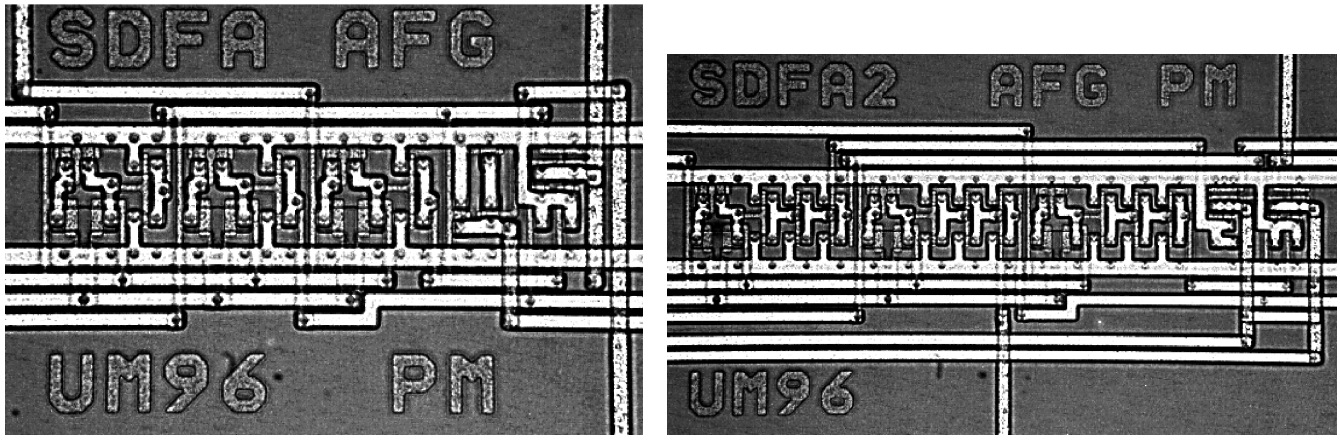
Fig. 12. Modifications for prototype implementation. (a) Modified circuit for generating *lit*1. (b) Detailed comparator circuit diagram.

cell which requires a reduced number of transistors by using the interim sum current generator which combines NMOS and PMOS transistors. In both versions of the prototype, inverters were replaced by voltage comparators, as described in the previous paragraph.

4.3 Experimental Results

Since the main objective of the prototype is to demonstrate the functionality of the SDFA cell, an experiment to show the transfer characteristics of the circuit was performed. These transfer characteristics were obtained by feeding the input of the circuit with a ramp signal of very low slew-rate. The experiment was done using the second version of the SDFA cell (Fig. 13b). The oscilloscope traces obtained in the experiment are shown in Fig. 14. In general, the form of the measured output functions agree with the expected circuit behavior shown in Fig. 11. Please note that the experiment is divided into two parts with respect to the value of $V_{\alpha_{i-1}}$. The trace labeled "V_{node}" reflects the operation of the RTD and corresponds to the expected behavior seen in Fig. 5c. Also note that the behavior of literal *lit*2 is independent of the value of $V_{\alpha_{i-1}}$. The last two traces show the transfer characteristics for the output functions, *w* and *c*, of the SDFA cell. Observe how the output characteristics are selected by $V_{\alpha_{i-1}}$.

There is a difference in the values of the output current levels between the measured characteristics and their expected



(a) (b)

Fig. 13. Microphotographs of the fabricated test chip.

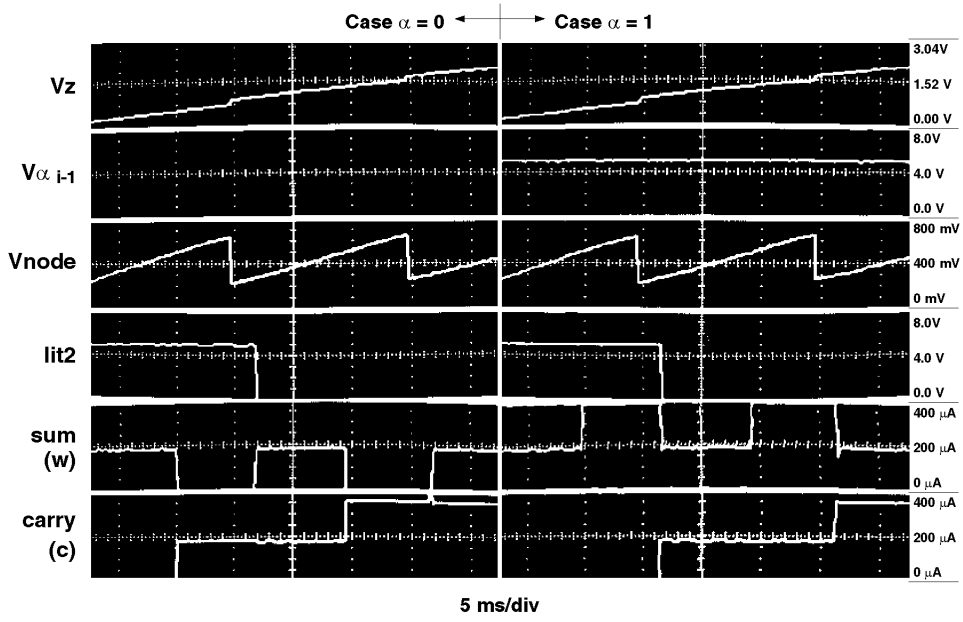


Fig. 14 Oscilloscope traces showing the operation of the signed-digit adder test circuit at low frequency.

values. While the expected output currents for logic levels "–1," "0," and "1" are 0.0, 0.5, and 1.0 milliampere, respectively, the measured current levels are 0.0, 0.2, and 0.4 milliampere (Fig. 14). This alteration of the current levels is due, in part, to a reduction in the transconductance of the PMOS devices—from 20.563 $\mu A/V^2$ in the SPICE model used for the simulations, to 16.129 $\mu A/V^2$ measured for the actual CMOS run of the test chips. Another reason for the difference in output levels is due to the method used for measuring the output currents. In the experiment, a resistive load was connected to the outputs in order to convert the current signals into voltage signals that could be displayed by the oscilloscope.

5 Conclusions

This paper presents a new multiple-valued signed-digit adder circuit that combines, for the first time, resonant-tunneling diodes (RTDs) with MOS field-effect transistors. RTDs provide high functionality for compact multiple-valued logic implementation, and MOS transistors enable efficient arithmetic circuit design through current-mode operation. The principle of operation of the proposed circuit was demonstrated using circuit simulation and also through a prototype fabrication where the GaAs-based quantum tunneling devices were not cointegrated with monolithically fabricated MOSFET devices. RTDs were externally added to verify the correctness of the SDFA operation as predicted by the simulation model.

The main advantage of the proposed design when compared to other redundant adder implementations is compactness, which is primarily due to the nonlinear characteristics of RTDs that enabled us to obtain three literal functions very efficiently. Also, current-mode of circuit operation, in which digits are summed by merely connecting their wires together [28], enabled us to reduce the transistor count. The number of devices is used as an estimate of the size of the circuit. This criterion is based on the fact that

TABLE 3
SDFA CELL COMPARED WITH OTHER IMPLEMENTATIONS

Design	Ref	Delay (ns)	Device Count
Redundant Binary Adder Cell	[3]	0.89	56
Current-Mode Multiple-Valued	[20]	7.0	34
Proposed SDFA		3.5	19

current technologies allow resistors with sizes equivalent to those of transistors. Using only 13 CMOS transistors, five resistors, and a two-peak RTD, the total number of active and passive devices used in the SDFA circuit is only 19.

The binary-valued counterpart of a radix-2 signed-digit adder is a redundant binary adder (RBA) cell usually implemented with CMOS logic. The functionality of the RBA cell is very similar to that of the signed-digit adder. The main difference is that the multivalued signed digits are represented by pairs of binary signals in the RBA cell. Many RBA designs have been developed, and constant refinements are being tried out to improve the performance. The fastest redundant binary adder cell is described in [3], which also presents a small survey of previous work on RBA cell designs. The compactness of the proposed signed-digit adder design compares very well against Makino's RBA cell that requires about 56 MOS transistors [3], as opposed to only 19 devices used in this paper. In terms of speed, however, the RBA cell implementation has an apparent advantage. The reported delay of the RBA cell is 0.89 nanosecond, while the proposed SDFA is estimated to have about 3.5 nanoseconds for the worst-case delay (see Table 2). This difference in speed performance is primarily due to the fact that our signed-digit adder was developed using a 2-micron CMOS process, while the results presented in [3] are based on a 0.5-micron process technology. Another current-mode, multiple-valued logic implementation of the radix-2 signed-digit adder cell was presented in [20] by Kawahito et al. Their signed digit adder uses 34 MOS transistors and has an estimated delay of 7 nanoseconds. Even though Kawahito et al. fabricated a prototype using a 10-micron process, the simulation-based delay estimation was obtained for a 2-micron process. Table 3 presents a comparison of the proposed signed-digit adder with other fast implementations of adder cells using both binary and multivalued logic.

Finally, this paper demonstrates that emerging quantum technologies which are going to be cointegrated with predominant semiconductor technologies such as CMOS, HBT, and HEMT will push the frontier of high-speed arithmetic and signal-processing VLSI circuits beyond the realm of conventional technologies. Resonant-tunneling devices, such as RTDs, RTBTs, RHEMTs, RHETs, etc., have several intrinsic advantages that can be exploited to design faster digital logic gates. Their nonlinear, folded-back characteristics will enable the circuit designers to implement complex functions very compactly. RTD's bistable property will be useful in building nanopipelined logic gates very easily, and its device speed and small capacitance will allow the designers to substitute RTDs for bulkier PMOS pull-up devices, thereby improving the circuit speed by dint of trimming down the load capacitances. Multivalued functions are also easy to implement by RTDs and this paper will encourage the researchers in the multivalued logic field to develop many other compact multivalued gates by using a combination of RTDs and conventional devices.

ACKNOWLEDGMENTS

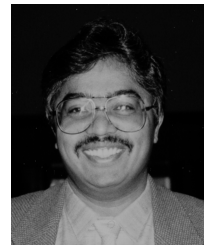
This work was supported by the U.S. Army Research Office under the MURI program, by DARPA, and by the U.S. National Science Foundation.

REFERENCES

[1] A. Avizienis, "Signed-Digit Number Representations for Fast Parallel Arithmetic," *IRE Trans. Electronic Computers*, vol. 10, pp. 389-400, Sept. 1961.
[2] S. Kawahito, M. Kameyama, T. Higuchi, and H. Yamada, "A 32 × 32-Bit Multiplier Using Multiple-Valued MOS Current-Mode Circuits," *IEEE J. Solid State Circuits*, vol. 23, pp. 124-132, Feb. 1988.
[3] H. Makino, Y. Nakase, H. Susuki, H. Morinaka, H. Shinohara, and K. Mashiko, "An 8.8-ns 54 × 54-Bit Multiplier with High Speed Redundant Binary Architecture," *IEEE J. Solid State Circuits*, vol. 31, pp. 773-783, June 1996.
[4] M. Kameyama, T. Seikibe, and T. Higuchi, "Highly Parallel Residue Arithmetic Chip Based on Multiple-Valued Bidirectional Current-Mode Logic," *IEEE J. Solid State Circuits*, vol. 24, pp. 1,404-1,411, Oct. 1989.
[5] M. Kameyama, M. Nomura, and T. Higuchi, "Modular Design of Multiple-Valued Arithmetic VLSI System Using Signed-Digit Number System," *Proc. Int'l Symp. Multiple-Valued Logic*, pp. 355-362, 1990.
[6] L.L. Chang, L. Esaki, and R. Tsu, "Resonant Tunneling in Semiconductor Double Barriers," *Applied Physics Letters*, vol. 24, pp. 593-595, 1974.
[7] N. Yokoyama, S. Muto, H. Ohnishi, K. Inamura, T. Mori, and T. Inata, "Resonant Tunneling Hot Electron Transistors (RHET)," *Physics of Quantum Electron Devices*, F. Capasso, ed., chapter 8, pp. 253-270. Springer-Verlag, 1990.
[8] A.C. Seabaugh, E.A. Beam, A.H. Taddiken, J.N. Randall, and Y.-C. Kao, "Co-Integration of Resonant Tunneling and Double Heterojunction Bipolar Transistors on InP," *IEEE Electron Device Letters*, vol. 14, pp. 472-474, Oct. 1993.
[9] G.I. Haddad, U.K. Reddy, J.P. Sun, and R.K. Mains, "Bound-State Resonant Tunneling Transistor (BSRTT): Fabrication, D.C. I-V Characteristics and High-Frequency Properties," *Superlattices and Microstructures*, vol. 7, no. 4, pp. 369-374, 1990.
[10] W.P. Dumke, J.M. Woodall, and V.L. Rideout, "GaAs-GaAlAs heterojunction Transistor for High Frquency Operation," *Solid State Electronics*, vol. 15, pp. 1,329-1,334, Dec. 1972.
[11] H. Kroemer, "Heterostructure Bipolar Transistors and Integrated Circuits," *Proc. IEEE*, vol. 7, pp. 13-25, Jan. 1982.
[12] R. Dingle, H.L. Störmer, A.C. Gossard, and W. Wiegmann, "Electron Mobilities in Modulation-Doped Semiconduction Heterojunction Superlattices," *Applied Physics Letters*, vol. 33, pp. 665-667, Oct. 1978.
[13] T. Mimura, S. Hiyamiza, T. Fujii, and K. Namba, "A New Field-Effect Transistor with Selectively Doped GaAs/n-Al$_x$GA$_{1-x}$As Heterojunctions," *Japanese J. Applied Physics*, vol. 19, pp. L22-L227, May 1980.
[14] T. Hanyu, Y. Yabe, and M. Kameyama, "Multiple-Valued Programmable Logic Array Based on a Resonant Tunneling Diode Model," *IEICE Trans. Electronics*, vol. E76-C, pp. 1,126-1,132, July 1993.

[15] K.C. Smith, "The Prospects for Multivalued Logic: A Technology and Application View," *IEEE Trans. Computers*, vol. 30, no. 9, pp. 619-634, Sept. 1981.
[16] A.C. Seabaugh, Y.-C. Kao, and H.-T. Yuan, "Nine-State Resonant Tunneling Diode Memory," *IEEE J. Solid State Circuits*, vol. 13, pp. 479-481, Sept. 1992.
[17] H.C. Lin, "Resonant Tunneling Diodes for Multi-Valued Digital Applications," *Proc. Int'l Symp. Multiple-Valued Logic*, pp. 188-195, 1994.
[18] T. Waho, "Resonant Tunneling Transistor and Its Application to Multiple-Valued Logic Circuits," *Proc. Int'l Symp. Multiple-Valued Logic*, pp. 130-138, 1995.
[19] L.J. Micheel and H.L. Hartnagel, "Intraband RTDs with nanoelectronic HBT-LED Structures for Multiple-Valued Logic Computation," *Proc. Int'l Symp. Multiple-Valued Logic*, pp. 80-85, 1996.
[20] S. Kawahito, M. Kameyama, and T. Higuchi, "Multiple-Valued Radix-2 Signed-Digit Arithmetic Circuits for High-Performance VLSI Systems," *IEEE J. Solid State Circuits*, vol. 25, pp. 125-131, Feb. 1990.
[21] U. König, M. Kuisl, J.-F. Luy, and F. Schäffler, "Si/SiGe Resonant Tunneling Devices Separated by Surrounding Polysilicon," *Electronic Letters*, vol. 25, pp. 1,169-1,171, 1989.
[22] U. König, M. Kuisl, F. Schäffler, G. Fischer, and T. Kiss, "Operating CMOS After a Si-MBE Process: A Precondition for Future Three-Dimensional Circuits," *IEEE Electron Device Letters*, vol. 11, pp. 218-220, May 1990.
[23] N. Evers, O. Vendier, C. Chun, M.R. Murti, J. Laskar, N.M. Jokerst, T.S. Moise, and Y.-C. Kao, "Thin Film Pseudomorphic A1As/InGaAs/InAs Resonant Tunneling Diodes Integrated onto Si Substates," *IEEE Electron Device Letters*, vol. 17, pp. 443-445, Sept. 1996.
[24] S.-J. Wei, H.C. Lin, R.C. Potter, and D. Shupe, "Dynamic Hysteresis of the RTD Folding Circuit and Its Limitation on the A/D Converter," *IEEE Trans. Circuits and Systems—II: Analog and Digital Signal Processing*, vol. 39, pp. 247-251, Apr. 1992.
[25] S. Mohan, J.P. Sun, P. Mazumder, and G.I. Haddad, "Device and Circuit Simulation of Quantum Electronic Devices," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 14, pp. 653-662, June 1995.
[26] S. Mohan, P. Mazumder, and G.I. Haddad, "NDR SPICE: A Circuit Simulator for Resonant Tunneling Devices," *Proc. Int'l Compound Semiconductors Conf.*, Sept. 1994.
[27] S. Mohan, P. Mazumder, and G.I. Haddad, "A New Circuit Simulator for Negative Resistance Devices," *Proc. Int'l Electron Devices Meeting*, Dec. 1994.
[28] M. Kameyama and T. Higuchi, "Design of a Radix-4 Signed-Digit Arithmetic Circuit for Digital Filtering," *Proc. Int'l Symp. Multiple-Valued Logic*, pp. 272-277, 1980.

Alejandro F. González (S'96) received the BE degree in electrical engineering (Licenciado en Ingeniería Electrónica) from the Instituto Tecnológico y de Estudios Superiores de Occidente, Guadalajara, Mexico, in 1993, and the MSE degree in electrical engineering from the University of Michigan, Ann Arbor, in 1995. He is currently pursuing the PhD degree in electrical engineering at the University of Michigan. His research interests include ultrafast digital circuit design, multiple-valued logic, and VLSI design automation. He is a student member of the IEEE.



Pinaki Mazumder (S'84–M'87–SM'95) received the BSEE degree from the Indian Institute of Science in 1976, the MSc degree in computer science from the University of Alberta, Canada, in 1985, and the PhD degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 1987.

For two years, he was a research assistant with the Coordinated Science Laboratory, University of Illinois at Urbana-Champaign. For more than six years, he was with Bharat Electronics Ltd. (a collaborator of RCA), India, where he developed analog and digital integrated circuits for consumer electronics products. During the summers of 1985 and 1986, he was a member of the technical staff in the Naperville, Illinois, branch of AT&T Bell Laboratories. He spent his sabbatical year as a visiting faculty member at Stanford University, University of California, Berkeley, and also at Nippon Telegraph and Telephone (NTT), Japan. He is presently a professor in the Department of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor. His research interests include VLSI testing, physical design automation, and ultrafast digital circuit design. He has written more than 100 papers for archival journals and international conference proceedings on these topics. He has coauthored two books entitled *Testing and Testable Design of Random Access Memories* (Kluwer, 1996) and *Genetic Algorithms for VLSI Layout and Test Automation* (Prentice Hall, 1998).

Dr. Mazumder was a recipient of Digital's Incentives for Excellence Award, U.S. National Science Foundation Research Initiation Award, and Bell Northern Research Laboratory Faculty Award. He is an associate editor of *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. He was a guest editor of *IEEE Design and Test*'s special issue on multimegabit memory testing, March 1993, a guest editor of *Journal of Electronic Testing: Theory and Applications*' special issue on advanced techniques for memory testing, April 1994, and a guest editor of *IEEE Transactions on VLSI Systems*' special issue on the impact of emerging technologies in VLSI systems, March 1998. He is a member of Sigma Xi, Phi Kappa Phi, the ACM Special Interest Group on Design Automation, and a senior member of the IEEE.