Multiple-Valued Logic in VLSI: Challenges and Opportunities

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Abstract

In recent years, there have been major advances in integrated circuit technology which have both made feasible and generated great interest in electronic circuits which employ more than two discrete levels of signal. Such circuits, called multiple-valued logic circuits, offer several potential opportunities for the improvement of present VLSI circuit designs. In this paper, we give an overview of recent developments in multiple-valued logic circuit design, revealing both the opportunities they offer and the challenges they face.

1 Introduction

When people ask me why I am doing research in multiple-valued logic, I often reply that it is like painting a picture having all possible colors available. Once you tried them, you will never return to just black and white. Multiple-valued logic displays us phenomena, we would never see in binary case, where the only two values available are *null* and *unit* elements of Boolean algebra[1], possessing very specific properties. Reflected back to two-valued scale, these phenomena give us a new, deeper understanding of the matter.

Apart from giving us a better insight into binary problems, multiple-valued logic has many other useful applications. They can be classified into two groups. The first group uses multiple-valued logic domain to solve binary problems more efficiently. For example, a well-known approach to represent a multiple-output Boolean function is to convert it to a single-output multiple-valued function, by treating its output part as a single multiple-valued variable. Such an approach is used, for instance, in Berkeley's tool for verification and synthesis VIS [1].

The second group targets the design of electronic circuits which employ more than two discrete levels of signals, such as multiple-valued memories, arithmetic circuits, Field Programmable Gate Arrays etc. Multiple-valued logic (MVL) circuits offer several potential opportunities for the improvement of present VLSI circuit designs. For example, serious difficulties with limitations on the number of connections of an integrated circuit with the

[1]The *null* **0** and *unit* **1** elements of an algebra over a set A have the properties that, for each $x \in A$, $x + \mathbf{0} = x$ and $x \cdot \mathbf{1} = x$

external world (pinout problem) as well as on the number of connections inside the circuit encountered in some VLSI circuit synthesis could be substantially reduced if signals in the circuit are allowed to assume four or more states rather than only two. In addition, there is a clear mathematical attraction of using multiple-valued number representation in many applications. For example, residue and redundant number systems allow to reduce or eliminate the ripple-through carries which are involved in normal binary addition or subtraction, resulting in high-speed arithmetic operations.

In spite of these potential advantages, practicality of MVL design heavily depends on the availability of circuit realizations, which must be compatible or competitive with present-day binary technologies. The purpose of this paper is to give the reader an overview of recent (1995-1999) developments in MVL circuit design, revealing both the opportunities they offer and the challenges they face. The earlier achievements in this area can be found in [3]-[5]. To achieve this goal in a reasonable space, we have had to exclude a number of topics which are of interest, but not central to our purpose. We do not deal with fuzzy logic, nor signal processing. Information about reliability or fault detection is excluded as is a whole range of purely theoretical material. Also, we do not discuss applications of multiple-valued logic to solving binary problems. A recent overview of this area can be found in [6]. Section 2 describes number representations alternative to binary. Section 3 shows possibilities for implementing multiple-valued circuits with integrated circuits technologies. Section 4 summarizes recent achievements in the design of MVL circuits. Section 5 concludes the paper.

2 Number Representation

A digital system represents information with discrete symbols rather than with continuously carrying quantity, as in a analog system. Digital binary systems use just two symbols, 0 and 1, to represent all information. Leaving aside for the moment the problem of circuit realization, we may ask whether the binary number representation is an optimum choice. The real world is not binary. It is more intuitive to reason about a system, especially at higher levels of abstractions, in terms of variables with symbolic values. In many practical engineering situations, a device can be not only in "off" or "on" state, but also in "idle" state. When arithmetic operations are involved, computing in a decimal system would match best our experience. In this section we discuss potential advantages of using multiple-valued number representation instead of binary one.

There are two major conventions for labeling values in a multiple-valued logic system over a set of m values. The most common is $0, 1, 2, \ldots, m-2, m-1$, extending binary notation in one direction only. It is called *unbalanced* (or *unsigned*, or *positive*). The second one requires an odd $m = 2r + 1$. It extends binary notation in both directions as $-r, 1-r, \ldots, -1, 0, 1, \ldots, r-1, r$. It is called *balanced* (or *signed*).

A string of digits $(a_{n-1} \ldots a_0)$ over a set of m values represents the number

$$a_{n-1}m^{n-1} + a_{n-2}m^{n-2} + \ldots a_0$$

For example, in the binary case of $m = 2$, $a_i \in \{0, 1\}$. In the ternary case of $m = 3$, $a_i \in \{0, 1, 2\}$ for the unbalanced system, and $a_i \in \{-1, 0, +1\}$ for the balanced system.

One concern in binary number representation is the treatment of negative numbers. There are three common techniques: (1) *sign-magnitude*, where a sign is explicitly attached to the front of the string of digits; (2) *1's complement*, where the representation for a negative number

is obtained by subtracting each digit from 1; (3) *2's complement*, where the representation for a negative number is obtained as in (2) but with a final addition of 1 to the number.

There are disadvantages of all three of these techniques. Both (1) and (2) have two representations for 0 (-0 and $+0$), while (3) permits the representation of one more negative number than positive. Alternatively, in a balanced system over a set of m values, all the numbers can be represented without using an explicit sign. The sign of a number is the sign of the most significant non-zero digit. Furthermore, in a ternary system, the negative of a number can be found by interchanging 1 and -1 throughout, leaving all zeros unchanged. Hence, addition and subtraction can be performed with the same hardware by sign changes of the addend and subtrahend, respectively, as required. One other advantage of a balanced system is that the procedure of rounding a number is identical to truncation. In a binary system it is not possible, because there is no way for negative correction being applied by digits of lower significance. Therefore, the correct value of the number must be approached from lower digits.

Another concern in binary number representation is that in performing addition (or subtraction), the sum bits depend on the carry form lower bits. Two alternative multiple-valued number systems have been extensively studied in order to reduce or eliminate the ripple-through carries. The first one is *residue* number system, in which there are no carries between bits. In such a representation, operations occur at each digit independently of the other digits, resulting in fast arithmetic operations [7], [8]. A disadvantage is that the size of the digits may vary, and thus different circuit designs might be needed for different digits.

The second number representation which has potential performance attractions is a number system with *redundancy*. In such a system, all numbers except 0 are not uniquely represented by a string of digits. Instead, two or more representations for a given number are available. The most significant digit does not depend on the least significant bit. The carry into a digit is computed only from (at most) the next two lower digits, but no other, enabling fast arithmetic operations. Multiple-valued arithmetic in redundant balanced number system [9], [10] as well as in redundant unbalanced number system [11], [12] have been presented.

Some other number representations which have potential advantages over binary have been studied, including overlap resolution number system based on signed continuous valued digits, allowing to perform arithmetic operations by analog digit manipulation circuitry [13] and redundant complex number system [14], allowing to perform addition and multiplication of complex numbers without treating real part and imaginary part separately as well as enabling carry-free addition and binary-tree multiple-operand addition.

3 Technology Considerations

Previous section shows that there is a clear mathematical attraction in the adoption of multiple-valued number representation. Its practicality, however, depends on the availability of circuit realizations, which must be compatible or competitive with present-day binary technologies. The attempts to built multiple-valued integrated circuits (ICs) of multiple-valued circuits compatible with IC technologies can be traced back to 1970, starting from the early works on 3-valued designs. Multiple-valued logic circuits have been implemented in bipolar technology, such as integrated injection logic (I^2L) and emitter-coupled logic (ECL); in complementary metal oxide semiconductor (CMOS) technology; in n-type MOS technology; and in charge-couple device (CCD) technology. Of the technologies applied, the two which show the greatest potential for commercialization are current-mode CMOS and quantum functional devices. In

this section, we briefly describe pro and contra of design of MVL circuits using these technologies.

3.1 CMOS current-mode MVL circuits

In current-mode circuits, currents are usually defined to have logical levels that are integer multiples of a reference current unit. Currents can be copied, scaled, and algebraically sign-changed with a simple current mirror. The frequently used linear sum operation can be performed simply by wiring, resulting in a reduced number of active devices in the circuit.

Several prototype chips of current-mode CMOS circuits have been fabricated, showing better performance compared to corresponding binary circuits ([7], [9], [11], [15], [16]). It is believed that current-mode designs can allow better noise margin than voltage-mode CMOS designs. Regrettably, the unique characteristics of CMOS binary logic, namely that of zero static power dissipation in either stable state, similar output impedance in either state are not carried over to MVL CMOS circuits. Instead, such circuits are usually characterized by rail-to-rail current flow in one or more static state and higher output impedance in one state compared to other states. Two solutions to these problems have been suggested recently. In [9], current-mode CMOS MVL circuits based on dual-rail source-couple logic have been introduced. The use of a complementary input pair and source-coupled logic allows high-speed circuits with low power dissipation. An alternative solution is proposed in [15], where low-voltage and low-power current-mode MVL circuits are designed using a neuron-MOS transistor.

Another problem with CMOS MVL circuits is that, unlike binary CMOS circuits, they are not self-restored. A level restorer circuit must be used every certain number of stages to recover the signal. To overcome this problem, a novel self-restored architecture has been recently presented [16]. It uses both current-mode MVL circuits and voltage-mode binary circuits to implement MVL functions and to restore output signal simultaneously. Binary gates are used within the design architecture so that MVL-binary or binary-MVL conversion circuits are not required to interface with binary circuits. The average size of the resulting circuits is about 50% smaller than previously proposed MVL circuits, while the average power dissipation and time delays are comparable.

3.2 MVL circuit design using quantum functional devices

An area of a special interest is implementation of MVL circuits using quantum functional devices. Negative-differential-resistance characteristics which appear in these devices have clear multiple threshold characteristics and therefore are very promising for MVL applications [10], [17]-[19]. Several MVL circuits have been constructed using resonant tunneling transistors (RTT) and resonant tunneling diodes (RTD) [20]-[24], or using surface tunneling transistors (STT) [25]. Although not at a mature stage yet, quantum devices may become indispensable for implementation of MVL circuits in the near future.

4 Design of MVL Circuits

The most promising applications of MVL are memories and arithmetic circuits, as we shall see in the sections that follow. Among other interesting recent achievements, not covered in this survey, are: MVL programmable devices [26]-[29], multiplexer [17], A/D converter [21], decoder [30], quantizer [20], and logic-in-memory VLSI structure [31].

4.1 Memories

In memory technology, recent applications of multiple-valued logic include Flash [32]-[37], DRAM [46], [47], CAM [40]-[42], and optical [43] memory designs. In what follows, we will concentrate on advances in Flash and DRAM memories, which seem to have the greatest commercial success. An overview of CMOS-related multiple-valued memory technologies can be found in [44] and of non-volatile multiple-valued memory technologies - in [45].

4.1.1 Flash memories

Flash memory is a non-volatile multiple-write EEPROM memory. Data is entered into the flash memory on a bit, byte, word or page boundary through programming. Once data is entered into the device it will remain, regardless of the presence or absence of power. Unlike traditional EEPROM, flash memory is limited in the granularity of the blocks that can be erased. The size of the erased blocks can range from 8Kbit to 1Mbit, depending on the product design. Array core cells of flash are normally arranged as NOR [32] or NAND [33] configurations. The memory cell consists of a single transistor with the addition of an electrically isolated polysilicon floating gate capable of storing charge (electrons). The single transistor memory cell results in a small cell size, and thus a small amount of silicon area is consumed for the storage of one bit of data, resulting in low cost.

The combination of non-volatility, electrical alterability and low cost makes flash memory attractive to small battery-powered systems. Flash memory devices are found in over 90% of PCs, over 90% of cellular phones and over 50% of modems. They are also key components of the emerging digital imaging and audio markets where it serves as the digital ”film” or digital ”tape”.

Traditionally, cost reduction and density increase for flash memory has been driven by process scaling in the same way as other semiconductor memory devices such as DRAMs and SRAMs. In 1992, Intel began a research effort to reduce the amount of silicon required to store a bit of data to a fraction of transistor through usage of multiple-valued logic and storing more than 1 bits of information per cell. The research resulted in manufacturing in 1997 64Mbit memory device StrataFlash storing two bits of information per cell [32]. Each cell consists of a single NOR transistor, implemented using 0.4μm ETOX flash memory process. The new device is just 5% larger than the 32MBit one bit per cell device. The double density is achieved maintaining the same 5V power supply and equivalent write performance. Read access time increased about 20%. The erase/write endurance specification is 10,000 cycles, which is 10 times less than the one of the one bit per cell product, but still more than acceptable for virtually all flash applications and easily justified by the reduced cost. Intel has also announced that they are planning to convert StrataFlash to a 0.25μm process in order to save costs, and starting the development of 0.18μm process technology [34].

Intel’s innovation was followed by a series of announcement of development of multi-level flash memories, competing with Intel’s device, including Samsung Electron’s 128Mbit 3.3V four-level NAND flash memory, fabricated with 0.4μm CMOS [35], Hitachi and Mitsubishi’s 256Mbit four-level NAND flash memory, fabricated with 0.26μm CMOS, NEC’s 64Mbit 3.3V four-level flash memory, based on 0.4μm CMOS and using Fowler-Nordheim (FN)-NOR type memory cell [37].

Another new idea, which is still in its infancy, is analog-based multiple-valued cell technology coming as a means of storing digitized data. Invox Technology has demonstrated that it can store three to four digital bits per cell after undergoing D/A conversion using NOR-

based flash memory device that can hold 256 levels of analog voltages in each cell [38]. This doubles the per-cell storage capacity of Intel's StrataFlash. Because it stores data in analog, Invox can stash charges in 12.5mV intervals in the floating gate of the flash cell transistor, and claims its technology can take it to 5mV resolutions. Invox targets applications which can tolerate some modifications to the original data, such as voice recorders, answering machines, cellular phone voice-mail recording and personal digital assistance.

Information Storage Devices (ISD) have also announced analog-based multiple-valued non-volatile memory technology, capable of storing 256 levels of analog voltage per cell and operating over a voltage range of 2.5V to 5.5V [39]. Additionally, it enables storage of voice and audio signals directly into memory, eliminating the need for analog-to-digital conversion. This does not only minimize, but also simplify the required external circuitry.

4.1.2 Dynamic RAM memories

DRAM memory is a volatile general purpose memory. A DRAM cell consists of a single capacitor and a single transistor. The capacitor stores a quantity of charge that corresponds to the logical value of the signal, and the transistor acts as a switch to transfer charge between the cell and the bit line when the cell is accessed. In conventional two-level storage, the signal charge is one-half the maximum stored charge, but in four-level storage, it is one-sixth [46]. Thus, to maintain the same signal level, the capacitance of a memory cell in the four-valued case should be three times larger than that in the binary case.

Density increase of DRAMs has been traditionally achieved by lithographic technology, permitting 70% reduction in the minimum design rule for each subsequent DRAM generation. Due to a combination of both design rule reduction and improvements in the call structure, the chip size has grown about 50% larger each generation, making the first 1Gbit DRAM reality in 1995. However, it was multi-valued storage technology that has allowed to push this density by a factor of 4 in just two years. In 1997 NEC has announced developing of a 4Gbit four-level DRAM, which is the densest semiconductor chip ever reported [47]. More than 2 billion memory cells are integrated on a single chip, with each cell storing 4-levels of charge (two bits of information). The four-level storage reduces the effective cell size by 50%. The capacitance of each memory cell is 60fF, achieved using a high-dielectric-constant material(Ba,Sr)TiO_3 as the memory cell capacitor dielectric. 4Gbit DRAM is fabricated with 0.15μm CMOS and has 2.0 - 2.5V power supply. Four-level sensing and restoring operations as well as time-shared sensing are used to increase speed and reduce sense-circuit area. A high data rate of 1.0Gbyte/s is achieved in 64Bit parallel-read mode.

4.2 Arithmetic circuits

In this section we describe recent achievements in the design of multiple-valued adders and multipliers. As we have noted in Section 2, residue and redundant number systems allow to reduce or eliminate the ripple-through carries which are involved in normal binary addition or subtraction, giving potential performance advantages.

4.2.1 Multipliers

The most convincing demonstration of the successful application of multiple-valued logic to the design of multipliers is 200 MHz 54×54-bit multiplier designed using multiple-valued current-mode MOS circuits [9]. The switching speed of the circuit is improved at a low 1.5V

supply voltage by using dual-rail source-couple logic, employing redundant balanced number representation, which results in a small signal-voltage swing while providing a constant driving current. The performance of the multiplier is evaluated to be about 1.4 times faster than that of a corresponding binary implementation under the normalize power dissipation. A prototype 4×4-bit multiplier chip was manufactured with 0.8μm standard CMOS technology with double metal layers and 1.7×1.4 mm^2 effective size.

In [12], another chip of a current-mode CMOS 4×4-bit quaternary multiplier was reported, fabricated using 0.8μm process and with 1.5×1.6 mm^2 core size. The high speed operation is achieved by direct generation of partial products using redundant number system. To add partial products in the multiplier, a redundant quaternary adder which can add two numbers without carry propagation is introduced. In the final level of addition, the resulting redundant numbers are converted to a non-redundant number by a high-speed quaternary carry-look-ahead adder.

A different design of a current-mode CMOS quaternary multiplier is reported in [48]. The circuit uses 49 MOS transistors, excluding bias generation circuitry and has the simulated worst case delay generating output currents about 10ms with 0.2μm CMOS technology.

Residue number system is employed in the multipliers described in [7] and [8]. [7] presents a modulo 7 multiplier using a barrel shifter and a sign inverter and composed of 60 transistors. The simulation results in 0.8μm CMOS technology and power supply 5V show delay time of 4.32ns. [8] presents an alternative design of a modulo m multiplier, with a delay time claimed to be proportional to $\log_2 m$.

4.2.2 Adders

In the design of multiple-valued adders, a recent achievement is the three-valued full adder circuit presented in [10]. The design is based on a multiple-valued literal circuit, utilizing negative differential resistance characteristics of RTDs to compactly implement its gated transfer function. MOS transistors are configured in current mode logic, where addition of two or more digits is achieved by superimposing the signals of individual wires being physically connected at the summing nodes. Redundant balanced number representation is used, allowing to perform addition of two arbitrary size binary numbers in constant time without the need for either carry propagation or carry look-ahead. The adder cell consists of 13 MOS transistors and one RTD, which is smaller that the state of the art CMOS redundant binary adder requiring 56 transistors [49]. Simulation results (using NDR-SPICE) show 3.5ns delay time, 3.5mW power dissipation, and noise margin of 0.15mA.

[50] presents a CMOS current-mode implementation of an MVL adder using differential logic circuit with dual-rail complementary inputs. The use of balanced redundant number representation results in a fast implementation at a 3.5V supply voltage. Simulation results based on 0.8μm CMOS process show 1.0ns delay time and 1.82mW power dissipation.

Residue number system is employed in the modulo 7 adder described in [7]. It is composed of 147 transistors. The simulation results in 0.8μm CMOS technology and power supply 5V show delay time of 7.49ns.

Some initial developments in the design of 7- and 10-valued adders, utilizing a unbalanced number representation, are presented in [11]. The first circuit is the 7-valued adder, fabricated in 0.8μm CMOS technology with a unit current step of 12μA. The second circuit is a decimal adder that uses a standard algorithm for adding decimal numbers, fabricated in 1.5μm CMOS technology with a unit current step of 1μA.

5 Conclusion

This paper has attempted to survey recent (1995-1999) developments in multiple-valued logic circuit design. The fact that some commercial products already benefit from multiple-valued logic is believed to be a first step towards recognition of the role of MVL circuits in the next generation of electronic systems.

A challenge to further utilization of multiple-valued logic in circuit design is creation of an effective computer-aided design package. Although some of the concepts and algorithms necessary for such a package have been already developed, a significant amount of research remains to be done.

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