Dynamic models for substrate coupling in mixed-mode systems

J.M.S. Silva and L. Miguel Silveira

Abstract: In modern monolithic integrated circuits, substrate coupling is a major concern in mixed-mode systems design. Verification of such systems implies the availability of accurate and simulation-efficient substrate coupling models. Traditionally, for frequencies up to a few gigahertz, pure resistive models have been considered sufficient. However, with increasing frequencies of operation, dynamic models become mandatory. The authors motivate the use of dynamic resistive-capacitive (RC) models of substrate coupling as a natural extension to the standard purely resistive models. They propose an extraction methodology that starts with information about the process parameters and circuit's contact layout, and leads to a contact-to-contact RC element model. The underlying algorithm is based on a finite difference discretisation of the substrate, leading to a large tridimensional mesh which is reduced by means of a fast multigrid algorithm. Unlike standard model order reduction algorithms which can produce models of similar accuracy to state-space descriptions, the proposed method leads to a realisable RC model that can trivially be incorporated into circuit simulation tools. As a first approximation, such a model is shown to correspond to a single time-constant system. Furthermore, it is shown that this time constant can be computed from knowledge of the conductivity and permittivity of a single dominant layer. It is verified that this formulation can accurately model substrate coupling effects for frequencies up to several tens of gigahertz.

1 Introduction

Substrate bulk behaviour in integrated circuits has long ceased to be considered as a perfect insulator $[1-3]$. As metal – oxide – semiconductor (MOS) transistor channel widths decrease to the size of a few nanometres, digital clock frequencies have been steadily increasing, so that current injection into the substrate as a result of fast-switching digital blocks becomes a great concern. Along with technology miniaturisation, die area has shrunk on behalf of package count and production yield purposes. Consequently, different cells and blocks are built closer to each other, in a way that facilitates injected substrate currents to migrate among the substrate layers and reach arbitrarily distant parts of the circuit $[3-5]$. This issue has mostly been a source of concern in the context of mixed-signal designs. Industry trends aimed at integrating higher levels of circuit functionality, resulting from an emphasis on compactness in consumer electronic products, and a widespread growth and interest in wireless communications, have triggered a proliferation of analogue– digital systems. The design of such systems is an increasingly difficult task owing to the various coupling problems that result from the combined requirements for high-speed digital and high-precision analogue components.

Analogue circuitry relies on accurate levels of currents and voltages, so that analogue transistors are correctly

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biased and projected performance is met. When substrate injected currents migrate through the substrate, substrate voltages fluctuate, causing havoc in sensitive analogue transistors, possibly leading to malfunctioning circuitry [3, 4, 6, 7].

Analysing the effects of substrate coupling requires that a model of such couplings is generated and used in a verification framework. Typically such a verification is done at the electrical level by means of a circuit simulator. An electric coupling model is generated and fed to a circuit simulator together with the remaining circuitry. Since potentially, everything couples to everything else through the common substrate, special care must be taken to make sure that the model is accurate but will not unnecessarily slow down the verification step. A common simplification is to assume that the major coupling mechanism is due to the finite resistivity of the substrate and then derive a resistive model. Such an approximation is considered valid whenever the dielectric relaxation time of the layers composing the substrate leads to an insignificant susceptance at the frequencies of interest. This approximation becomes questionable beyond a few gigahertz, specially since harmonics of significant amplitude, generated by circuit nonlinearities, may fall in the range of frequencies where reactive effects are of importance.

A methodology is proposed for generating dynamic resistive-capacitive (RC) models of substrate coupling. Unlike standard model order reduction algorithms which can produce models of similar accuracy to state-space descriptions, the proposed method leads to a realisable RC model that can trivially be incorporated into circuit simulation tools. The methodology proposed for model extraction is detailed and the model is analysed in terms of its validity and accuracy. In Section 2, the mechanisms for substrate coupling are briefly discussed and background work

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in this area is reviewed. In Section 3, starting from information about the process parameters and circuit's contact layout, a contact-to-contact RC element model is derived. As a first approximation, such a model is shown to correspond to a single time-constant system. Furthermore, we show that this time-constant can be computed from knowledge of the conductivity and permittivity of a single dominant layer. In Section 4 the model's validity, accuracy and relevance is discussed through some example simulations. To verify our model, we also compare it to one obtained using standard model order reduction techniques, and show it to be of similar accuracy. Finally in Section 5 some conclusions are drawn.

2 Background

2.1 Substrate coupling mechanisms

Coupling through the substrate occurs, mainly, because of substrate finite resistivity. Devices built into the same substrate are consequently not perfectly isolated from each other. Considering a typical substrate profile like the one shown in Fig. 1, MOS transistors are based on channel formation so substrate resistivity is not desired to be infinite. Latch-up avoidance considerations also support a similar argument. However, when a transistor is on, while current flows through the corresponding channel, part of it is injected into the substrate and is free to migrate to arbitrarily distant substrate zones. At higher frequencies, when active areas are charged and discharged, source-bulk and drainbulk parasitic capacitances show a low impedance and current is directly injected into the substrate by these active areas. In reality, recent studies have shown that, because of package parasitics, noise at the supply lines are the major contributors to substrate-coupled disturbances, both at the digital and at the analogue ends [8]. Supply lines interact with the substrate mainly through the substrate contacts of both the circuit core and the ring of pads and inject currents into the substrate. The fact that such currents are in a sense free to roam around the substrate and may be captured wherever appropriate conditions are met, makes the verification process much harder. While it is true that most of the coupling may occur locally, designer experience and good design practices lead to designs where such local couplings are explicitly minimised. As a consequence, the assumption of mostly local coupling is not necessarily valid and unexpected long range couplings may appear where least expected. As such, not only is it mandatory that some kind of substrate model be used to account for substrate couplings between different devices

which also have low simulation costs [4, 6, 7, 9, 10]. These models are, however, generally very imprecise. Furthermore, heuristic models are only really useful to the designer, for they are unable to account for higher order effects and, in fact, rely on designer's experience to prune out the expected relevant couplings [11]. Moreover, once that is accomplished they do not provide any form of veri-

On the other hand, methodologies that avoid a priori heuristic pruning and work at the electrical level directly are typically based on a full description of the media and all the possible couplings. A problem that arises from model extraction in those cases is the extraction time and the size of the final model. Coupling can occur from any substrate contact to any other, so that a full interaction matrix can be drawn from it. Several methods have been proposed to generate such a model. Boundary element methods (BEM) are one of these families of methods. In BEM, only the surface of the substrate contacts is discretised which leads to a system of equations that corresponds to small but full matrices. Extraction of such models requires intensive computations which restricts the range of applicability of this method to small to medium sized circuits $[12-14]$. Fortunately, significant progress in BEM performance has been achieved $[15-17]$. A different family of extraction methods is finite difference (FD) or finite element methods (FEM). In these methods, the whole 3D volume of the substrate is discretised leading to larger but sparse matrices. The relative complexity of each type of methods is hard to predict as it depends on the particular discretisation algorithm used. In a BEM, if the substrate top surface is covered with N_s nodes, a fast solver will require $\mathcal{O}(N_s \log N_s)$ operations to generate a model. For an FD method with a similar number of nodes on the surface, the total number of unknowns is approximately $M_v = N_s^{3/2}$ (assuming a cubic volume with a similar discretisation). In this case, fast solution techniques have a complexity of $\mathcal{O}(M_v)$ [17-23]. The number of nodes required by each method is however very problem-dependent. It is therefore also problem-dependent which method provides the better solution, computationally wise.

built on the same substrate, but that model must also account for all or at least large portions of the substrate.

Several extraction methodologies were studied in the past and, based on them, several extracting tools were developed. The simplest modelling methodologies consist of finding coupling elements based on heuristic rules. Such methods are very attractive since the extraction overhead is minimal and they lead to simple first-order models

fication as to whether the performed approximation enables

2.2 Previous work

correct circuit simulation.

In this work, a method for the extraction of RC models is proposed and its usefulness and validity are assessed. As mentioned previously, RC models of substrate coupling are less commonly used than purely resistive models. Notwithstanding, previous work has been published in this field that considers the needs for capacitive effects in substrate coupling $[18, 23-28]$. In some of these works, reasonable assumptions about layout and substrate geometries are made $[25, 27]$. In our work, we use FD and make no geometrical approximations, accounting for accuracy. RC models are also partially used in some commercial tools, typically in an heuristic way, but there is no systematic assessment of their relevance. In [28], higher order RC

3 Substrate coupling dynamic model extraction

In this section, we propose an extraction methodology leading to a circuit-level, dynamic, contact-based model of the couplings through the substrate.

3.1 Finite difference tridimensional model

In order to derive a model of the substrate coupling, the substrate is first assumed as a layered medium (recall Fig. 1). In our extraction method we use an FD technique to discretise the substrate volume, accounting for accuracy. This implies a discretisation of the substrate volume into a large number of small cuboid elements. It is known that FD discretisation provides increasing accuracy as the discretisation spacing tends to zero. An example of such a discretisation is shown in Fig. $2a$ where the nodes of the 3D mesh are visible. Clearly, in practice more elaborate meshing algorithms should be used in order to place more grid nodes near the regions of interest.

Starting from Maxwell's equations and neglecting the effect of magnetic fields, we use the identity $\nabla(\nabla \times a) = 0$ and Ampére's law in each cuboid element (node), to write

$$
\nabla J + \frac{\partial}{\partial t} \nabla D = 0 \tag{1}
$$

where J is the current density and D is the electric displacement. Equation (1) is the continuity equation and expresses the conservation of electric charge. Recalling that $J = \sigma E$ and $D = \varepsilon E$ where σ and ε are the conductivity and the permittivity of the medium, respectively, and E is the electric field, (1) can also be written as

$$
\sigma \nabla E + \varepsilon \frac{\partial}{\partial t} \nabla E = 0 \tag{2}
$$

As the substrate is spatially discretised, Equation (2) can be solved with a simple box integration technique. Assuming an homogeneous medium in each substrate layer, we

Fig. 2 Finite difference method a Substrate discretisation b Substrate resistive-capacitive model

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consider a cuboid whose centre is node i with neighbour cuboid whose centre is node *j*. If E_{ii} denotes the electrical field normal to the cuboid side surface between nodes i and j, the FD approximation leads to

$$
E_{ij} \simeq \frac{V_i - V_j}{l_{ij}} \tag{3}
$$

where l_{ij} is the distance between adjacent nodes i and j, and V_i and \dot{V}_j are the scalar potentials at those nodes.

From the divergence theorem, we know that

$$
\int_{\mathcal{S}_i} E \, \mathrm{d}\mathcal{S}_i = \int_{\mathcal{V}_i} \nabla E \, \mathrm{d}\mathcal{V}_i \tag{4}
$$

where V_i is the volume of the *i*th cuboid and S_i its surface. Assuming that the electric field is constant in each surface of the cuboid and its gradient is also constant in the cuboid's volume, (4) becomes

$$
\sum_{j} E_{ij} S_{ij} = \nabla E V_i \Leftrightarrow \nabla E = \frac{1}{V_i} \sum_{j} E_{ij} S_{ij} \tag{5}
$$

where the summation is performed on cuboids that are neighbours of cuboid *i*, and S_{ij} is the common surface between cuboids i and j . This approximation is valid if the discretisation is accurate enough (virtual infinitesimal cuboids).

The above derivation assumed a common resistivity, that is, a single layer. The extension to multiple layers is trivially handled by making sure that the layer interface is filled with cuboids and by either appropriately averaging or weighting the different layer resistivities in the computations for the cuboids at the interfaces. Replacing (3) and (5) into (2), results in

$$
\sum_{j} \left[G_{ij}(V_i - V_j) + C_{ij} \left(\frac{\partial V_i}{\partial t} - \frac{\partial V_j}{\partial t} \right) \right] = 0 \tag{6}
$$

where $G_{ij} = \sigma S_{ij}/l_{ij}$ and $C_{ij} = \varepsilon S_{ij}/l_{ij}$. Equation (6) can readily be interpreted in terms of the electrical model depicted in Fig. $2b$. In fact, applying nodal analysis (NA) to the 3D mesh model (6) leads to the following system of equations

$$
(sC + G)V = I \tag{7}
$$

where C and G are, respectively, the capacitance and conductance matrices of the system, V is the voltage on all nodes of the discretisation mesh and I is the corresponding injected currents. From (6) , entries in G and C in (6) , corresponding to nodes residing in a given layer, can be approximated with the well-known formulas

$$
R_{ij} = \rho \frac{S_{ij}}{l_{ij}} = \frac{1}{\sigma} \frac{S_{ij}}{l_{ij}}
$$

$$
C_{ij} = \varepsilon \frac{S_{ij}}{l_{ij}}
$$
 (8)

here applied to each element in the model.

The size of the model in (7) is directly determined by the chosen discretisation. For very fine discretisations the model in (7) could be very large indeed. On the other hand, one should note that this model is sparse, since matrices C and G correspond to the 3D discretisation stencil and have at most seven non-zero entries in each row or column.

Typical extraction methodologies note that the substrate relaxation time is negligible for frequencies up to a few

gigahertz [20], and thus proceed to ignore the capacitive portion of the model. In the following, we will retain the full model from (6) and discuss its computation and relevance. Note however that the basic assumptions made during the above derivation, starting from (1), limit the applicability of the modelling procedure to frequencies up to tens of gigahertz. Beyond that, a full electromagnetic model is required [27].

3.2 Circuit-level contact-based model extraction

Using the 3D mesh model from (6) in any electrical simulator is prohibitive, as the number of circuit nodes is too large. As such, a reduced model must be sought. A possible solution to this problem is to apply standard model order reduction (MOR) techniques to the problem and obtain a reduced model $[29-31]$. For such methods, the size of the resulting model is directly proportional to the product of the approximation order by the number of ports (inputs and outputs, or contacts in our case). This causes two potential problems. First, an appropriate reduction order must be devised. Second, for systems with large numbers of contacts, small increases in the approximation order lead to large increases in model size and potentially to overly large models. Furthermore, application of MOR techniques leads to a mathematical model description, such as a rational function representation. Not all simulators can efficiently handle such descriptions directly, particularly if the number of ports is large. Incorporating such a model in a standard environment requires an additional realisation step, whereby a circuit that has a similar time-domain response is derived. Here we propose a constructive methodology and seek to obtain a simple realisable RC model directly, as depicted in Fig. 3 for a three-contact setup. In the proposed strategy, model size is uniquely determined by the number of substrate contacts and thus independent from the chosen discretisation or any other parameter. Furthermore, we note that this model is an obvious extension of the typical resistive models whereby a coupling resistance is computed between pairs of contacts [22]. Here, that resistance is replaced with the parallel impedance of a resistor and a capacitor. Assuming a model similar to that of Fig. 3, but generalising to any number of contacts, and using NA, the corresponding system of equations is given by

$$
\boldsymbol{Y}_c(s)\boldsymbol{U} = (s\boldsymbol{C}_c + \boldsymbol{G}_c)\boldsymbol{U} = \boldsymbol{J} \tag{9}
$$

where Y_c is the admittance of the contact's system, C_c and G_c are, respectively, the capacitive and resistive coupling elements between contacts, and U and J are the vectors of contact voltages and injected currents. This system is analogous to (7) but much smaller, its size being determined by the number of contacts and therefore independent of the discretisation.

The phasor representation of (9) can be expressed as

$$
(j\omega C_c + G_c)\bar{U} = \bar{J}
$$
 (10)

where \bar{U} and \bar{J} are, respectively, the voltage and current phasors.

If the imposed voltage in contact k is \overline{U} such that $U_k = 1 \times \sin(j\omega t + 0)$ and all other components are 0, then, in (10), \bar{J} will equal the kth column of $G_c + j\omega C_c$. Therefore given \bar{U} with the particular form chosen, determining the corresponding \vec{J} gives us one column of the model. Using appropriate vectors for \bar{U} , specifically setting in turn each contact voltage to 1 V and the remainder to 0 V, we can repeat this process as many times as the number of contacts so that the full admittance matrix $Y_c = G_c + j\omega C_c$ is formed, one column at a time. For each choice of \bar{U} , the result \bar{J} is a complex vector, whose real part can directly be interpreted as a resistive term, whereas the imaginary part, normalised by ω , can be interpreted as a capacitive term. Therefore the desired realisable RC model can be directly and trivially inferred from the computations described. The cost of computing this contact model, $Y_c(i\omega)$, for a system of m contacts is thus equal to *m* times the cost of determining J given some U . Fortunately this computation can be performed on the 3D mesh in a straightforward way. To simplify the description and without loss of generality, consider the three-contact system depicted in Fig. 3 for which we want to compute the admittance description, that is (10). The inputs to this system are thus the voltages imposed at the contacts $[U_1,$ U_2 , U_3]. In the extraction methodology proposed, after discretisation, a system such as (7) is obtained. Setting a contact's voltage to some value is equivalent to setting the voltages of all nodes in the mesh that correspond to that contact to that value (recall that contacts have volume and therefore each contact may correspond to several mesh nodes). In our case, this can be written as $V = M[U_1, U_2,$ U_3 ^T, with $M \in \mathbb{R}^{n \times 3}$ being an appropriate contact incidence matrix. Lines in \overrightarrow{M} correspond to mesh nodes, whereas columns correspond to contacts. Inspection of column k of M reveals that $M_{pk} = 1$ if node p is in contact k , 0 otherwise. Since NA is used, the inputs to (7) should be currents, applied to nodes adjacent to the contact nodes. The values of such currents can easily be obtained from the corresponding Norton equivalent circuits seen by those nodes. Fig. 4 depicts such a transformation assuming that node k is contained in one such contact and node p , one of its neighbours in the grid, is not a member of any contact. The complete transformation can be written as

$$
I = Y_{\text{adj}}[U_1, U_2, U_3]^{\text{T}}
$$
 (11)

where I is the vector of injected currents on all nodes of the 3D mesh, and $Y_{\text{adj}} \in \mathbb{C}^{n \times 3}$ is a matrix, combining the incidence matrix \overrightarrow{M} mentioned above, relating the sources applied to the contacts to the mesh nodes, and the Norton equivalent admittances seen by the nodes in the mesh that are adjacent to those contacts. Clearly, most of the lines

Fig. 3 RC model for three-contact configuration Fig. 4 Norton equivalent for resistive-capacitive models

of matrix Y_{adj} are zero. Indeed, the only exceptions are entries in the matrix occurring at lines corresponding to the nodes adjacent to the contacts.

On the other hand, the output of the system is given by the current on the contacts $[J_1, J_2, J_3]$. Combining (7) with (11) , it is easy to see that these can be obtained as

$$
\begin{bmatrix} J_1 \\ J_2 \\ J_3 \end{bmatrix} = \boldsymbol{Y}_{\text{adj}}^{\text{T}} \boldsymbol{V} = \boldsymbol{Y}_{\text{adj}}^{\text{T}} (\boldsymbol{G} + j\omega \boldsymbol{C})^{-1} \boldsymbol{Y}_{\text{adj}} \begin{bmatrix} U_1 \\ U_2 \\ U_3 \end{bmatrix} \quad (12)
$$

which exposes the admittance of our simplified two-contact system. Obviously this derivation extends trivially to the generic m contacts case leading to

$$
J = Y_{\text{adj}}^{\text{T}} V = \underbrace{Y_{\text{adj}}^{\text{T}} (G + j\omega C)^{-1} Y_{\text{adj}}}^{T} U \qquad (13)
$$

where now $J = [J_1, \ldots, J_m]$ and $U = [U_1, \ldots, U_m]$ and Y_{adj} would now take into account all contacts in the problem. Equation (13) clearly exposes the desired admittance contact model. From (13) , given U , it is conceptually trivial to obtain J for any given frequency, ω . This procedure can then be used to compute J given a particular U , in a constructive, column by column manner, as described.

Two issues remain to be discussed. The first one relates to the solution of (12) at a given frequency, which involves the large, yet sparse G and C matrices. Fortunately this can be performed very efficiently by means of a fast multigrid algorithm with a cost of $O(n)$ per solve, albeit here using complex arithmetic. For details see [21, 22]. The second issue relates to an appropriate choice of the frequency ω at which the solution is computed. This is a more insidious issue, with implications at many levels. We will address this issue in an heuristic manner in the following section. We should point out, however, that there is a critical implicit approximation being made in the procedure proposed. While the computation of the model's admittance matrix has been performed at a given frequency, ω , the model is then assumed to be valid for all frequencies. That is, even though we solve (7) for an appropriately chosen single ω , once we interpret the result as an RC network, the model is equivalent to (9). An obvious consequence of this fact is that the model will behave as a single time-constant network, with a time-constant directly related to ω . This is of course an approximation that requires a good choice of the time-constant. However, we have seen, and experiments corroborate this idea, that there is indeed a dominant timeconstant in such a layered three-dimensional discretised medium. We will attempt to provide further justification for this conjecture in ensuing sections.

The full algorithm to perform dynamic substrate coupling full-model extraction is presented in Algorithm 1. Not surprisingly, this is the obvious extension of the standard procedure used nowadays to obtain resistive models[18, 21, 22].

Algorithm 1: Admittance model extraction algorithm

Given the technology layer information, determine an appropriate frequency for the system formulation and then, for every contact, k :

1. Put nodes on contact k at a predetermined voltage of 1 V;

2. Using Norton's equivalent, obtain the currents injected into adjacent nodes;

3. Solve the 3D system (7) obtaining all nodes voltages, V ;

4. From V and the 3D model admittances, use Ohm's law to compute the node injected currents, J ;

5. Use Gauss' law and sum injected node currents to obtain contact injected currents, J;

6. By (9) and as only nodes on contact k have a non-zero voltage, the kth column of $G_c + C_c$ equals J.

3.3 Heuristic determination of single time-constant model

To motivate our choice of the frequency ω for which the system equations are formulated, we start by looking into a simplified setting. Single layer substrates, although perhaps, from an industry standpoint, interesting only for cost reasons, have several characteristics which are useful when studying RC model properties. On a single layer silicon medium, generic elements in G and C satisfy, respectively, the following relations

$$
\frac{c_{ij}}{g_{ij}} = \frac{\varepsilon S_{ij}/l_{ij}}{\sigma S_{ij}/l_{ij}} = \frac{\varepsilon}{\sigma} \equiv \alpha \tag{14}
$$

and thus

$$
C = \alpha G \tag{15}
$$

throughout. Therefore $s\mathbf{C} + \mathbf{G} = (\alpha s + 1)\mathbf{G}$. It is also trivial to see that in this case $Y_{\text{adj}} = sY_{\text{adj}_c} + Y_{\text{adj}_g} = (\alpha s + 1)Y_{\text{adj}_g}$, where Y_{adj_c} and Y_{adj_g} correspond to, respectively, the capacitive and conductive parts of the Norton equivalent (see Fig. 4 for a depiction). Replacing in (13)

$$
J = Y_{\text{adj}}^{\text{T}}(\boldsymbol{G} + s\boldsymbol{C})^{-1} Y_{\text{adj}} \boldsymbol{U}
$$

= $(\alpha s + 1) Y_{\text{adj}_s}^{\text{T}} \frac{1}{\alpha s + 1} \boldsymbol{G}^{-1} (\alpha s + 1) Y_{\text{adj}_s} \boldsymbol{U}$
= $(\alpha s + 1) Y_{\text{adj}_s}^{\text{T}} \boldsymbol{G}^{-1} Y_{\text{adj}_s} \boldsymbol{U}$ (16)

Recalling that computation of J above, with appropriate U , produces a column of $Y_c(s) = sC_c + G_c$, then two conclusions immediately become evident. First, that computation of J using (16) can be performed by solving a real system of equations, instead of a complex one, followed by multiplication by a complex number. Second, that the conductance contact coupling matrix, G_c , can be obtained column by column, as discussed previously, and C_c is simply obtained by multiplying G_c by α , that is

$$
C_c = \alpha G_c \tag{17}
$$

Therefore with a single solve in real arithmetic, the reduced RC model in (9) can be obtained for single layer substrate profiles (in fact, we need to perform as many solves as the number of contacts, but that is the exact same cost of generating a resistive-only model). Furthermore, (17) shows that the branch relation from the 3D model in (14) carries over to the contact model. What is perhaps more interesting is that (16) also shows that the contact model is a single time-constant model, α . Contrasting this fact with the methodology proposed previously, it becomes obvious that for this particular setting, the approximate model computation proposed can be made exact with the choice $\omega = 1/\alpha$. Therefore for single layer isotropic substrates, we have shown that the system behaves as a single time-constant system and, furthermore, that the timeconstant is given by σ/ε , the layer relaxation time or intrinsic time-constant.

For substrates with multiple layers, different ratios will be obtained for (14), depending on the layer under consideration. In this case, the derivation in (16) is still generically valid, if α is interpreted as a matrix of size equal the number of nodes on the 3D mesh, whose entries are dependent upon the level in which each mesh node is located. However, computational handling of α in this case is cumbersome and does not provide much insight into the proper choice α

As we will see in the following section, multiple-layer substrates naturally show higher order behaviour, that is, involving more dynamic content. Notwithstanding, its behaviour in the frequencies of interest, which range from DC to a few dozen of gigahertz, is still 'first order', that is, dominated by a single time-constant. As such we propose an alternative heuristic approach by which an appropriate frequency is chosen. For higher frequencies, more dynamic features are exhibited, but for lower frequencies one can see the effect of a dominant admittance 'corner' frequency which is now determined by the properties of the top layer where the contacts are contained, namely its conductivity, σ_1 . When the frequency of the signal is such that $\omega > \sigma_1/\varepsilon$, its intrinsic admittance starts to increase, turning into a very low impedance path between contacts, and eventually dominating the overall admittance. We propose to use such value as the frequency ω for which the system (16) is solved, so that the single time-constant model follows the corner of the admittance curve. Therefore we can use the described first-order model for multiple-layer technologies with satisfying accuracy.

There are several ways in each we can fit a first-order model to the exact admittance behaviour between contacts, and contacts and backplane. In fact, depending on what one wants to minimise, several options are available. For instance, we could match the asymptotic behaviour, by matching the admittance characteristic both at DC and at infinity, and perhaps allowing the model to be less accurate in the medium cutoff frequencies. To obtain such a model we could match the DC response by solving for the conductive part of the model, in essence getting the usual resistive-only model. Then, to get a capacitive counterpart for the model, one could perform a very similar system solution, but this time considering all conductances as being capacitances. This is equivalent to a solve for the complete system for very high frequencies, at which the conductive component of the admittance is neglectable comparing to the capacitive part (i.e. the high-frequency asymptotic behaviour). Such a model requires therefore two solves in real arithmetic. In this method, the admittance characteristic is matched both at DC and at infinity, but may show a large error in the intermediate range of frequencies, namely around the 'first corner', related to the cutoff frequency of the top layer. Since we contend that such frequency is related to the dominant time-constant of the system, being inaccurate in this range is not such a good idea.

An alternative method, which we call restrictivedynamic, is to first generate the resistive part of the model, thus matching DC, and then generate the capacitive part by simply scaling the conductance part, according to the cutoff frequency of the top layer, as in the single-layer case. As we shall see, this will produce a model that only matches the first cutoff frequency with a first-order model. Therefore the model will unavoidably show growing error as more of the system dynamics come into play (i.e. after the following cutoff frequencies, corresponding to the other layers, become relevant). Still it will be, by construction, accurate in the low-frequency regime up to the range where capacitive effects start to come into play. Fortunately this is exactly the desired behaviour we seek for our model.

3.4 Model order reduction

A different way of obtaining a circuit-level contact-based model is to apply model order reduction (MOR) techniques directly to the system in (7) resulting from the 3D discretisation and specifying the order of the reduced model to be obtained. This can be efficiently done with several known methods, for instance with PRIMA [31] which is a MOR method based on block Arnoldi orthogonalisation [32]. The PRIMA procedure starts from the equations describing the 3D formulation, namely

$$
sCV + GV = Y_{\text{adj}}U
$$

$$
J = Y_{\text{adj}}^{\text{T}}V
$$
(18)

Using a block Arnoldi procedure, a basis for the Krylov subspace involving C, G and Y_{adi} can be constructed. If N is the matrix whose columns span the Krylov subspace of order p , then a p-order reduced model can be computed in the following way

$$
(N^{T}CN)sV = -(N^{T}GN)V + N^{T}Y_{\text{adj}}U
$$

\n
$$
J = Y_{\text{adj}}^{T}NV
$$

\n
$$
\Leftrightarrow
$$

\n
$$
s\tilde{C}_{r}V = -\tilde{G}_{r}V + \tilde{Y}_{\text{adj}}U
$$

\n
$$
J = \tilde{Y}_{\text{adj}}^{T}V
$$
\n(19)

The reduced model can thus be obtained as

$$
\boldsymbol{J} = \tilde{\boldsymbol{Y}}_{\text{adj}}^{\text{T}} (\tilde{\boldsymbol{G}}_r + s\tilde{\boldsymbol{C}}_r)^{-1} \tilde{\boldsymbol{Y}}_{\text{adj}} \boldsymbol{U}
$$
 (20)

which bears an obvious resemblance to (13) . An important difference, however, is that the model generated by MOR techniques is the state-space representation given by (19) which may not be easy to include in a standard simulation environment. To avoid this problem, one would have to realise an RC network whose equations would match (19). While this is not such a hard task, it may lead to a cumbersome network, with controlled sources connecting the internal states to the ports (because of \tilde{Y}_{adj} realisation), a situation that can lead to unforeseen difficulties in the timedomain simulation, resulting from scaling problems and asymmetries.

3.5 Computational complexity

When discussing the computational cost of modelling substrate coupling, we must distinguish between two different tasks: the model generation and the model evaluation. Model generation is the task of creating the model, either using the approach proposed, standard model order reduction algorithms, or any other appropriate technique. Model evaluation refers to the cost of direct model evaluation, for computing the model outputs given its inputs, either in the frequency domain (for instance to generate a Bode plot) or in the time domain. The complexity of model evaluation is also sometimes discussed when referring to the added cost of using a substrate model during verification, usually in a circuit simulation context. Table 1 summarises the computational cost of both model generation and evaluation in terms of the relevant parameters.

Table 1: Computational complexity of model generation and evaluation in terms of the number of contacts, m, model order, q, and number of FD discretisation nodes, n

	Model generation	Model evaluation
Full (3D)		$O(n^s)$
PRIMA	$O(qmn^s)$	$O(qm^3)$
Resistive-dynamic	$\mathcal{O}(mn^s)$	$\mathcal{O}(m^3)$

s is a small constant depending on the technique used

For most algorithms that we discussed, including the proposed algorithm, model generation requires multiple solves with the original system. For the single time-constant model proposed, exactly one matrix solve per contact is needed to compute the model. This is exactly the same cost incurred by computing a first-order model using an algorithm such as PRIMA. Therefore in terms of computational cost, both techniques are equivalent. Higher-order PRIMA models can be computed but the model generation cost will increase accordingly. Furthermore, the size of the model will also increase which will impact model evaluation. Since large matrices are involved in these computations, the cost of model generation is usually fairly high. Still this situation is tacitly accepted since it is recognised that this cost can later be amortised if the model is to be reused many times.

For model evaluation, the cost is a function of the size and sparsity of the model. The full 3D model, albeit being very large, is quite sparse and the cost of its evaluation can be estimated as $O(n^s)$, a low polynomial in *n*, the number of nodes in the 3D grid (e.g. $n^{1.5}$ when using standard Cholesky). Direct analysis of (13) indicates that the size of the model generated by the proposed approach is the number of contacts. Furthermore, as Fig. 3 indicates, the model is full, indicating that there is a network element between every pair of terminals. A similar situation is seen if a first-order PRIMA model is used. Evaluation of the model requires manipulation of a full $m \times m$ matrix, which implies cubic cost. Therefore simulation either in the frequency domain at a given frequency or in the time domain at a given timepoint is cubic in the model size (higher-order models generated with PRIMA will have proportionally higher size).

It is known that the cost of circuit simulation is usually superlinear in the number of equations. This is in fact the reason why the full 3D model is never used, as the number of volume nodes in the substrate could easily overwhelm the total number of circuit unknowns and dominate the total cost. For our single time-constant model, addition of the substrate model adds as many new nodes as contacts in the model. This implies that simulation of a circuit with the substrate model will be more expensive. Not only can the number of nodes almost double, by adding a contact per device, as the substrate model, being a dense model, will greatly increase the total cost. This situation also happens when generating a model with PRIMA, as the model will also be full and of size proportional to the number of inputs. A penalty of one order of magnitude or more has been reported in this case. To avoid this problem sometimes heuristic techniques are used in order to prune the number of elements in the model, thus reducing the model size. In either case, the cost of model evaluation is cubic in m , the number of substrate contacts (typically $m \ll n$).

When considering substrate coupling, one must be clearly aware that the cost of verification could greatly increase. Still, the added accuracy is definitely worth the trouble for sensitive or leading designs.

4 Substrate coupling dynamic model validation

In this section, we analyse some characteristics of the single time-constant model and validate its applicability. In Section 4.1, we start by estimating the range of frequencies for which dynamic models become necessary. Then in Section 4.2 we validate the proposed model by comparing it to the original unreduced system from Fig. $2b$. We reason from the 3D model to show that the proposed model, as a first approximation, corresponds to a single time-constant system. Furthermore, we show that this timeconstant can be computed from knowledge of the conductivity and permittivity of a single dominant layer. Finally in Section 4.3, we show, through a simple simulation example, the accuracy of the proposed model.

4.1 Relevance of dynamic model component

In order to evaluate the importance of capacitive coupling through the substrate we can look at, for instance, the 3D model of Fig. $2b$) or, equivalently, at (16). Considering any branch in the circuit representing the discretisation, dynamic effects will become relevant when the susceptance of the capacitor becomes comparable to the conductance of the parallel resistor. Clearly this depends upon the frequencies of operation given that for low frequencies the susceptance is negligible. Assuming that the capacitive part becomes relevant when the susceptance reaches for instance 10% of the conductance, we have

$$
\omega C_{ij} \ge 0.1 G_{ij} \Leftrightarrow \omega \varepsilon \frac{S_{ij}}{l_{ij}} \ge 0.1 \sigma \frac{S_{ij}}{l_{ij}} \Leftrightarrow \omega \ge 0.1 \frac{\sigma}{\varepsilon} \quad (21)
$$

Applying this result to a technology of a single-layer substrate with $\rho = 15$ Ocm and $\varepsilon_r = 11.9$ (cf. Fig. 5), the previous equation leads to $\omega = 6.327 \text{ grad/s} \Leftrightarrow f \simeq 1 \text{ GHz.}$ This confirms the usual assumption about the validity of resistive models for frequencies up to a few gigahertz, depending on the technology.

In single-layer substrates the contact model must, as was shown in the previous section, confirm the previous result. Table 2 lists values extracted using the method proposed for a simple configuration such as shown in Fig. 6. In this experiment, a discretisation of $257 \times 129 \times 257$ cuts in x, y and z, respectively, was used.

Taking, for instance, the values of R_{12} and C_{12} of Table 2, and assuming the same error factor of 10%, we have

$$
\omega C_{12} \geq 0.1 G_{12} \Leftrightarrow \omega \geq 6.327 \text{ grad/s} \Leftrightarrow f \simeq 1 \text{ GHz}
$$
 (22)

Fig. 5 Typical substrate doping profiles (sizes in μ m) Relative permittivity of the medium is $\varepsilon_r = 11.9$ a High resistivity substrate

b Low resistivity substrate with high resistivity epitaxial layer

Table 2: Resistance and capacitance values for dynamic model for a three-contact configuration on a single-layer substrate

Contact 1	Contact 2	Resistance, $k\Omega$	Capacitance
	backplane	13.26	1.192 fF
		180.7	87.47 aF

This result, at the contact level and using extracted data, is compatible with the result at the 3D model mesh level, as expected. It serves as additional validation for the extracted model values. Clearly, for frequencies upward of a few gigahertz, a purely resistive model will be inaccurate as it will not take into account the increase in admittance because of the susceptance term. The above result should in fact be obvious in light of the derivation in Section 3.3 where it was proved that, for single-layer substrates, the basic relation that exists between the capacitive and conductive terms in all branches of the 3D model carries over exactly to the contact model.

Interestingly enough, however, very similar results are obtained for technologies with two-layer substrates, as we shall see in the following.

4.2 RC model accuracy

As seen in the previous section, for frequencies greater than a few gigahertz, it becomes necessary to use dynamic coupling models. The model proposed attempts to fulfill that need but it is necessary to verify its accuracy and limitations.

Several experiments have been elaborated using typical substrate doping profiles, like those presented in Fig. 5. The contact layout used in these experiments is shown in Fig. 6. Properties of the system (13), like pole and zero location, pole residues, Bode plots and so on, were studied.

We have already seen in Section 3.3 that in single-layer isotropic substrates the system has a single admittance zero. This is because of the 3D system having all poles and zeros clustered around a specific frequency, corresponding to the single intrinsic time-constant of the layer, given by σ/ε . In multiple layer substrates, each layer possesses a different intrinsic time-constant. However, it turns out that a very similar behaviour still occurs. For higher frequencies, more dynamic features are exhibited, but for lower frequencies one can see the effect of a dominant admittance 'corner' frequency which is now determined by the properties of the top layer where the contacts are

Fig. 6 Contact layout used in the experiments (units in μ m) Contacts have a depth of $2 \mu m$

Error for entry ij of model Y is defined with respect to the full 3D model, \mathbf{Y}^{3D} , as err(\mathbf{Y}_{ij}) = max{| $\mathbf{Y}_{ij} - \mathbf{Y}_{ij}^{3D}$ |/| \mathbf{Y}_{ij}^{3D} |}

contained. As suggested in Section 3.3, when the frequency of operation is such that $\omega > \sigma_{epi}/\varepsilon$, the intrinsic admittance of the top layer, $y_{ij}^{(top)} = g_{ij}^{(top)} + j\omega c_{ij}^{(top)}$, starts to increase, turning into a very low impedance path between contacts, and eventually dominating the overall admittance. In our experiments, the resistive-dynamic reduced model parameters were obtained by solving (7) once for $\omega = 0$, in order to obtain G_c with high accuracy, and then setting $C_c = \varepsilon / \sigma_{\text{eni}} G_c$, corresponding to the intrinsic cutoff frequency of the top layer.

As expected, for the single-layer profile both methods produce the same model which is quite accurate (see Table 3 where the maximum relative error of entry ij of

Fig. 7 Magnitude and phase Bode diagram of admittance between contact and backplane for 3D transfer function and proposed models for substrate profile from Fig. 5b

a Magnitude of admittance between one contact and the backplane b Phase of admittance between one contact and the backplane

Fig. 8 Magnitude and phase Bode diagram of admittance between contacts for 3D transfer function and proposed models for substrate profile from Fig. 5b

a Magnitude of admittance between contacts

b Phase of admittance between contacts

model Y, defined against the full 3D model, Y^{3D} , as $err(Y_{ij}) = max\{|Y_{ij} - Y_{ij}^{3D}|/|Y_{ij}^{3D}|\}$, is presented). In the twolayer case, the lower layer shows a resistivity lower than the top layer, and as the contacts are immersed in the top layer, it is that one which dictates the cutoff frequency. For the asymptotic model described in Section 3.3, two solves were performed, one for $\omega = 0$ to obtain G_c , and another for $\omega \rightarrow \infty$ to obtain C_c , which means neglecting the real components of the 3D elements and solving the resulting system.

In Figs. 7 and 8, we show the magnitude and phase Bode plots obtained with the full 3D model and the proposed resistive-dynamic reduced model for the admittances

Table 4: Maximum relative error for dynamic model for a two-contact configuration on a two-layer substrate, varying the distance between contacts

d	Resistive-dynamic	
	$err(\boldsymbol{Y}_{11})$	$err(\boldsymbol{Y}_{12})$
98	5.895 \times 10 ⁻⁶	9.203×10^{-6}
8	3.065×10^{-6}	7.257×10^{-6}
2	1.781×10^{-6}	2.796×10^{-6}

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Table 5: Maximum relative error for dynamic model for a two-contact configuration on a two-layer substrate, varying the size of the contacts

a	Resistive-dynamic		
	err (Y_{11})	err (Y_{12})	
0.2	3.915×10^{-6}	5.730 \times 10 ⁻⁶	
2	5.895×10^{-6}	9.203×10^{-6}	
20	9.801×10^{-6}	1.484×10^{-5}	

Table 6: Maximum relative error for dynamic model for a two-contact configuration on a two-layer substrate, varying the depth of the epitaxial layer

Fig. 9 Magnitude Bode diagram of 3D transfer function and proposed models for substrate profile from Fig. 5b with $D = 4 \mu m$ a Admittance between one contact and the backplane b Admittance between contacts

Fig. 10 Simulation circuit and layout a Test circuit b Contact layout

between one contact and the backplane, and between two contacts. Both in magnitude and in phase the approximations are indistinguishable, which shows that the proposed model has very good accuracy throughout the frequency range of interest, accurately capturing the dynamics around the dominant pole/zero until around a hundred of gigahertz. Furthermore, the plot also shows quite effectively the limits of using both a purely resistive model for substrate coupling, as well as using the asymptotic model. In fact, the asymptotic model shows low error for $\omega = 0$ and $\omega \rightarrow \infty$ but is unable to accurately model the admittance behaviour in the relevant frequencies.

We have repeated the above experiments with a variety of contact configurations by changing the contacts distance, contact sizes and epi-layer depth. The corresponding results are presented in Tables 4, 5 and 6 and show the maximum relative error in the frequency range from DC to 10^{12} rad/s \simeq 159 GHz. As can be seen from the tables, the single time-constant model can accurately model the behaviour of the impedance between both contacts (Y_{12}) , and between the contacts and the backplane (Y_{11}) . The resistive-dynamic model shows a low error even in the case of $D = 4 \mu m$, where the distance between contacts is much larger that the depth of the epitaxial layer (cf. Fig. 9 for the corresponding magnitude Bode plots; we have omitted the phase plots because of space constraints and since they added little to the discussion). This happens because in typical substrate profiles with two layers the resistivity of the bulk is always much lower than the resistivity of the epitaxial layer. Consequently, the time-constant inherent to the bulk manifests itself several orders of magnitude after the cutoff frequency of the epitaxial layer.

4.3 Resistive-capacitive model simulation

In order to assert the importance of dynamic substrate models in circuit simulation, a simple experimental configuration was designed (cf. Fig. 10). Three complementary MOS (CMOS) inverters connected to one another were laid

Fig. 11 Sensor's bulk node

Fig. 12 Sensor's drain voltage fluctuation

a Drain voltage of sensor

b Detail of drain voltage of sensor

out next to an 'analogue' transistor. The three CMOS inverters are meant to inject noise into the substrate which will be sensed by the n-type MOS (NMOS) transistor, m_7 . A substrate coupling model between all contacts has been extracted. In the simulation phase, the chain of inverters was driven by a 1 GHz non-ideal square-wave, with rise and fall times of around 1 ps, and the noise injected through the NMOS channel areas of the inverters was coupled to the sensitive m_7 bulk. The sensor transistor has been biased such that its drain voltage is constant and around 0.5 V in perfect isolation conditions. Figs. 11 and 12 show the waveforms of the voltages in the bulk and drain of the sensing transistor, respectively, in three different situations: when using no substrate coupling model, when using purely resistive coupling models and when using the proposed RC coupling model. For validation of the results obtained with the proposed model, we are also showing the results obtained when using a PRIMA-generated model (since using the full 3D mesh would be computationally too expensive).

These are however indistinguishable from the proposed model results. As it can clearly be seen in the figures, the injection of noise into the substrate by the inverters makes substrate voltage fluctuate and, thus, through the body effect of m_7 , its drain voltage also fluctuates. The results obtained with the dynamic models (our proposed RC model and the PRIMA model) show significantly more dynamics during the transients than those obtained with the straightforward resistive-only model, including strong coupling spikes that may cause undesired behaviour. Clearly the difference from resistive to RC models is that resistive models do not account for substrate intrinsic capacitance properties, which at higher frequencies enhance coupling effects. Therefore the dynamic models are able to show more accurately the effects of substrate coupling. Resistive models are therefore unable to predict correct functioning of the 'analogue' transistor.

5 Conclusions

A methodology for the extraction of realisable dynamic RC substrate coupling models that naturally extends the traditional resistive-only modelling techniques has been presented. Reduced models obtained for a formulation based on an FD discretisation were computed using a fast multigrid algorithm and are shown to offer high accuracy for a large spectrum of frequencies. The model produced is a fairly accurate first-order approximation, as checked by comparison with another model of similar accuracy computed with standard MOR techniques. It has been experimentally verified by simulation that the full 3D mesh substrate model presents an admittance characteristic which shows a dominant zero at σ_1/ε where σ_1 is the conductivity of the top layer where the contacts are immersed, and ε is the permittivity of the medium. The proposed dynamic model is computed at such a frequency in order to minimise transfer function and numerical errors. Extensive experiments and simulations of a simple example circuit performed using the proposed model demonstrate both its relevance and its accuracy for frequencies up to several tens of gigahertz.

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7 References

- 1 Joardar, K.: 'A simple approach to modeling cross-talk in integrated circuits', *IEEE J. Solid-State Circuits*, 1994, 29, (10), pp. 1212–1219
- 2 Kup, B.M.J., Dijkmans, E.C., Naus, P.J.A., and Sneep, J.: 'A bit-stream digital-to-analog converter with 18-b resolution', IEEE J. Solid-State Circuits, 1991, 26, (12), pp. 1757–1763
- 3 Gharpurey, R.: 'Modeling and analysis of substrate coupling in integrated circuits'. PhD dissertation, Department of Electrical Engineering and Computer Science, University of California at Berkeley, Berkeley, CA, June 1995
- Su, D.K., Loinaz, M.J., Masui, S., and Wolley, B.A.: 'Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits', IEEE J. Solid-State Circuits, 1993, 28, (4), pp. 420–430)
- 5 Verghese, N.: 'Extraction and simulation techniques for substrate-coupled noise in mixed-signal integrated circuits'. PhD dissertation, Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA, August 1995
- 6 Johnson, T.A., Knepper, R., Marcellu, V., and Wang, W.: 'Chip substrate resistance modeling technique for integrated circuit design', IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., 1984, 3, (2), pp. 126– 134
- Nauta, B., and Hoogzaad, G.: 'How to deal with substrate noise in analog CMOS circuits'. European. Conf. on Circuit Theory and Design, Budapest, Hungary, September 1997, Late 12:1-6
- Aragones, X., and Rubio, A.: 'Experimental comparison of substrate noise coupling using different wafer types', IEEE J. Solid-State Circuits, 1999, 34, (10), pp. 1405– 1409
- 9 van Genderen, A.J., van der Meijs, N.P., and Smedes, T.: 'Fast computation of substrate resistances in large circuits'. European Design and Test Conf., Paris, February 1996, pp. 560-565
- Mitra, S., Rutenbar, R.A., Carley, L.R., and Allstot, D.J.: 'A methodology for rapid estimation of substrate-coupled switching noise'. IEEE 1995 Custom Integrated Circuits Conf., 1995, pp. 129–132
- 11 Phillips, J.R., and Silveira, L.M.: 'Simulation approaches for strongly coupled interconnect systems'. Int. Conf. on Computer Aided-Design, November 2001, pp. 430 –437
- 12 Smedes, T., van der Meijs, N.P., and van Genderen, A.J.: 'Extraction of circuit models for substrate cross-talk'. Int. Conf. on Computer Aided-Design, San Jose, CA, November 1995, pp. 199–206
- 13 Gharpurey, R., and Meyer, R.G.: 'Modeling and analysis of substrate coupling in integrated circuits'. IEEE 1995 Custom Integrated Circuits Conf., 1995, pp. 125– 128
- 14 Verghese, N.K., and Allstot, D.J.: 'SUBTRACT: a program for the efficient evaluation of substrate parasitics in integrated circuits'. Int. Conf. on Computer Aided-Design, San Jose, CA, November 1995
- 15 Costa, J.P., Chou, M., and Silveira, L.M.: 'Efficient techniques for accurate modeling and simulation of substrate coupling in mixed-signal IC's'. Design, Automation and Test in Europe, Exhibition and Conf., Paris, France, February 1998, pp. 892-898
- 16 Chou, M., and White, J.: 'Multilevel integral equation methods for the extraction of substrate coupling parameters in mixed-signal IC's'. 35th ACM/IEEE Design Automation Conf., June 1998, pp. 20–25
- 17 Kanapka, J., Phillips, J., and White, J.: 'Fast methods for extraction and sparsification of substrate coupling'. Proc. 37th ACM/IEEE Design Automation Conf., June 2000
- 18 Clement, F.J.R., Kayal, E.Z.M., and Declercq, M.: 'Layin: toward a global solution for parasitic coupling modeling and visualization'. Proc. IEEE Custom Integrated Circuit Conf., May 1994, pp. 537–540
- Wemple, I.L., and Yang, A.T.: 'Mixed-signal switching noise analysis using Voronoi-tesselation substrate macromodels'. 32nd ACM/IEEE Design Automation Conf., San Francisco, CA, June 1995, pp. 439–444
- 20 Stanisic, B., Verghese, N.K., Rutenbar, R.A., Carley, L.R., and Allstot, D.J.: 'Addressing substrate coupling in mixed-mode IC's: simulation and power distribution systems', IEEE J. Solid-State Circuits, 1994, 29, (3), pp. 226–237
- 21 Silveira, L.M., and Vargas, N.: 'Characterizing substrate coupling in deep sub-micron designs', IEEE Des. Test Comput., 2002, 19, (2), pp. 4–15
- 22 Silva, J.M.S., and Miguel Silveira, L.: 'Substrate model extraction using finite differences and parallel multigrid', Integr. VLSI J., 2007, 40, pp. 447 –460
- 23 Chen, T.-H., Luk, C., and Chen, C.C.-P.: 'SuPREME: substrate and power-delivery reluctance-enhanced macromodel evaluation'. Int. Conf. on Computer Aided-Design, San Jose, CA, November 2003, pp. 786–792
- 24 Gharpurey, R., and Hosur, S.: 'Transform domain techniques for efficient extraction of substrate parasitics'. Proc. Int. Conf. on Computer-Aided Design, November 1997, pp. 461-467
- 25 Pfost, M., and Rein, H.-M.: 'Modeling and measurement of substrate coupling in si-bipolar IC's up to 40 ghz', IEEE J. Solid-State Circuits, 1998, 33, (4), pp. 582–591
- 26 Lan, H., Yu, Z., and Dutton, R.W.: 'A CAD-oriented modeling approach of frequency-dependent behavior of substrate noise coupling for mixed-signal IC design'. Fourth Int. Symp. on Quality Electronic Design, 2003, March 2003, pp. 195–200
- 27 Li, H., Carballido, J., Yu, H.H., Okhmatovski, V.I., Rosenbaum, E., and Cangellaris, A.C.: 'Comprehensive frequency-dependent substrate noise analysis using boundary element method'. Int. Conf. on Computer-Aided Design, San Jose, CA, November 2002, pp. 2 –9
- 28 Xu, C., Fiez, T., and Mayaram, K.: 'High Frequency Lumped Element Models for Substrate Noise Coupling'. IEEE Int. Workshop on Behavioral Modeling and Simulation, October 2003, pp. 47–50
- 29 Feldmann, P., and Freund, R.W.: 'Efficient linear circuit analysis by Padé approximation via the Lanczos process', IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., 1995, 14, (5), pp. 639–649
- 30 Silveira, L.M., Kamon, M., and White, J.K.: 'Algorithms for coupled transient simulation of circuits and complicated 3-D packaging', IEEE Trans. Compon. Packag. Manuf. Technol. B, Adv. Packag., 1995, 18, (1) , pp. $92-98$
- 31 Odabasioglu, A., Celik, M., and Pileggi, L.T.: 'PRIMA: passive reduced-order interconnect macromodeling algorithm', IEEE Trans. Comput.-Aided Des., 1998, 17, (8), pp. 645–654
- 32 Grimme, E.: 'Krylov projection methods for model reduction'. PhD dissertation, Coordinated-Science Laboratory, University of Illinois at Urbana-Champaign, Urbana-Champaign, IL, 1997