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Publicações

Capítulos em Livros

[1] Luís Miguel Silveira. Modelos de ordem reduzida para interligações em sistemas electrónicos. In Ricardo Reis, Sandro Sawick, and Rafael Santos, editors, *Advanced Topics on Microelectronics*, Série Inovação, pages 109–120. Doravante Publishers, London, U.K., April 2006.

[2] João M. S. Silva and L. Miguel Silveira. Dynamic models for substrate coupling in mixed-mode systems. In Manfred Glesner, Ricardo Reis, Leandro S. Indrusiak, Vincent Mooney, and Hans Eveking, editors, *VLSI-SoC: From Systems to Chips*, volume 200/2006 of *IFIP International Federation for Information Processing*, pages 21–37. Springer Boston, Boston, MA U.S.A., August 2006.

[3] João M. S. Silva, Jorge Fernandez, Paulo Flores, and L. Miguel Silveira. Outstanding issues in model order reduction. In Gabriela Ciuprina and Daniel Ioan, editors, *Scientific Computing in Electrical Engineering*, volume 11 of *Mathematics in Industry*, pages 139–152. Springer Berlin Heidelberg, May 2007.

[4] João M. S. Silva and L. Miguel Silveira. Issues in model reduction of power grids. In R. Reis, A. Osseiran, and H. Pfleiderer, editors, *VLSI-SOC: From Systems to Silicon*, volume 240/2007 of *IFIP International Federation for Information Processing*, pages 127–144. Springer Boston, Boston, MA U.S.A., October 2007.

[5] Luís G. Silva, Zhenhai Zhu, Joel R. Phillips, and L. Miguel Silveira. Library compatible variational delay computation. In G. de Micheli, S. Mir, and R. Reis, editors, *Research Trends in VLSI and Systems on Chip*, volume 249/2008 of *IFIP International Federation for Information Processing*, pages 157–176. Springer Verlag, Boston, MA U.S.A., November 2007.

[6] Joel R. Phillips, Zhenhai Zhu, and L. Miguel Silveira. PMTBR: a family of approximate principal-components-like reduction algorithms. In W. H. A.Schilders and H. A. van der Vorst, editors, *Model Order Reduction: Theory, Research Aspects and Applications*, Mathematics in Industry, pages 111–132. Springer Boston, Berlin, Germany, May 2008.

Artigos em Revistas Internacionais

[1] Joel R. Phillips and L. Miguel Silveira. Poor Man's TBR: A simple model reduction scheme. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 24(1):43–55, Jan. 2005.

[2] L. Miguel Silveira and Joel R. Phillips. Resampling plans for sample point selection in multipoint model order reduction. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 25(12):2775–2783, December 2006.

[3] Carlos P. Coelho, Joel R. Phillips, and L. Miguel Silveira. Generating high-accuracy simulation models using problem-tailored orthogonal polynomials basis. *IEEE Transactions on Circuit and Systems I: Fundamental Theory and Applications*, 53(12):2705–2714, December 2006.

[4] João M. S. Silva and L. Miguel Silveira. Dynamic models for substrate coupling in mixed-mode systems. *IET Circuits, Devices & Systems*, 1(3):221–232, June 2007.

[5] João M. S. Silva and L. Miguel Silveira. Substrate model extraction using finite differences and parallel multigrid. *Integration, the VLSI Journal, Elsevier Publishing*, 40(4):447–460, July 2007.

[6] P. Flores, H. Neto, and J. Marques-Silva. Generating realistic stimuli for accurate power grid analysis. *submitted to TODAES - ACM Transactions on Design Automation of Electronic Systems*, 2008.

Artigos em Conferências Internacionais

[1] Luís G. Silva and L. Miguel Silveira. Grid-based statistical timing analysis. In *Proceedings of the IADIS International Conference on Applied Computing*, pages 73–80, Algarve, Portugal, February 2005.

[2] João M. Silva and L. Miguel Silveira. Issues in model reduction of power grids. In *VLSI-SoC'2005 - IFIP International Conference on Very Large Scale Integration*, pages 127–144, Perth, Australia, October 2005.

[3] José C. Monteiro, Jorge R. Fernandes, and L. Miguel Silveira. A case for a triangular waveform clock signal. In *VLSI-SOC'2005 XIV IFIP International Conference on VLSI*, pages 72–77, Perth, Australia, October 2005.

[4] L. Miguel Silveira. Outstanding issues in model order reduction. In *International Conference on Scientific Computing in Electrical Engineering*, pages 108–109, Sinaia, Romenia, September 2006.

[5] Luís G. Silva, Joel R. Phillips, and L. Miguel Silveira. Variation-Aware, Library Compatible Delay Modeling Strategy. In *Proceedings of the 14^{th} IFIP WG 10.5 International Conference on Very Large Scale Integration and System-on-Chip*, pages 122–127, October 2006.

[6] Luís G. Silva, Joel R. Phillips, and L. Miguel Silveira. Efficient computation of the exact worst-delay corner. In *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, pages 1617–1622, February 2007.

[7] Luís G. Silva, Joel R. Phillips, and L. Miguel Silveira. Efficient computation of the worst-delay corner. In *DATE - Design, Automation and Test in Europe, Exhibition and Conference*, Nice, France, April 2007.

[8] W. H. A. Schilders, W. Schoenmaker, and L. M. Silveira. Coupled simulations in the modeling of complete nanoscale rf blocks. In *International Conference on Computational Methods for Coupled Problems in Science and Engineering*, Ibiza, Spain, May 2007.

[9] Jorge Ferñandez Villena, Wil H. A. Schilders, and L. Miguel Silveira. Parametric structure-preserving model order reduction. In *VLSI-SOC'2007 XVI IFIP International Conference on VLSI*, pages 31–36, Atlanta, Georgia, U.S.A., October 2007.

[10] João M. Silva and L. Miguel Silveira. On the effectiveness of reducing large linear networks with many ports. In *International Symposium on Circuits and Systems*, pages 2694–2697, New Orleans, Louisiana, USA, May 2007.

[11] João M. Silva and L. Miguel Silveira. On the compressibility of power grid models. In *IEEE International Symposium on VLSI*, pages 186–191, Porto Alegre, RS, Brazil, May 2007.

[12] Pedro M. Morgado, Paulo F. Flores, and L. Miguel Silveira. Generating realistic stimuli for accurate power grid analysis. In *IEEE International Symposium on VLSI*, pages 233–238, Porto Alegre, RS, Brazil, May 2007.

[13] João M. Silva, Joel R. Phillips, and L. Miguel Silveira. Efficient representation and analysis of power grids. In *DATE - Design, Automation and Test in Europe, Exhibition and Conference*, pages 420–425, Munich, Germany, March 2008.

[14] Jorge Ferñandez Villena and L. Miguel Silveira. Spare: a scalable algorithm for passive, structure preserving parameter-aware model order reduction. In *DATE - Design, Automation and Test in Europe, Exhibition and Conference*, pages 586–591, Munich, Germany, March 2008.

[15] P. Marques Morgado, Paulo F. Flores, José C. Monteiro, and L. Miguel Silveira. Generating worst-case stimuli for accurate power grid analysis. In *Proceedings of the 2008 PATMOS Workshop (to be published by Springer in Lecture Notes for Computer Science)*, Lisbon, Portugal, September 2008. Springer-Verlag.