A Case for a Triangular Waveform Clock Signal

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Abstract

In this paper we argue that global synchronization can be achieved using a triangular waveform with advantages at many levels. The smoothness of the waveform (hence, lower frequency components) translates into significantly lower power consumption and induced noise when compared with a square clock signal. Additionally, given its linear variation with time, time references can be defined not only by the period of the clock signal, but by the varying voltage level of the triangular waveform. This feature allows for the reduction of the triangular signal frequency, hence further reducing the noise and minimizing clock signal degradation. The proposed triangular waveform can be used for chip-wide clock distribution, from which a square waveform can be extracted locally, permitting existing modules to be used without alterations, thus avoiding any shift from standard design styles.

1. Introduction

The continuing development in technology has led to an ever decreasing feature size in VLSI circuits, which permits a larger number of active elements in a single circuit, operating at higher frequencies. The up side is that more and more complex functionality can be accommodated in a single chip. The down side is that there are a set of new issues that have to be dealt with in order to exploit this potential to the fullest.

Today, the amount of active elements available allow for the design of entire systems on a single chip (SoC) [1]. In general, these circuits are composed of a set of modules which communicate synchronously with each other. A special signal, the clock signal, is used to synchronize the operations among the modules in the circuit. Typically, the clock signal is a square waveform. A rising (or falling) edge serves as a time reference, indicating that all the computations of the previous time-slot have completed and that their results are ready to be used in a new computation.

The reduction of feature size, which translates to smaller capacitances that need to be charged or discharged, allows for the increase in clock frequency, an offer designers are eager to adopt. However, as the clock frequency increases, so does:

- the power consumption [2];
- the problems related to clock skew, clock jitter and clock reflection [3];
- the noise induced by the clock signal [4].

Given the importance of the clock signal in VLSI circuits and the problems raised by the increasing clock frequency, a significant amount of research work has been put into developing methodologies for the optimization of clock distribution [5].

In this paper, we argue that global synchronization can be achieved using a triangular waveform with advantages at many levels. A triangular waveform presents a much smoother variation over time than a square wave, which means frequency components with much lower amplitude, and lower current spikes. This translates into significantly lower power consumption and lower induced noise. Furthermore, since voltage varies linearly with time, time references can be determined not only by the period of the clock signal, but also by voltage levels of the triangular waveform. Hence, in one clock period of the triangular waveform, several time-slots can be defined, allowing for a much lower frequency for the clock signal.

An apparent disadvantage of a triangular over a square waveform is the lower slope of the signal at the transition point, which could potentially make it more sensitive to jitter problems. However, we note that, with todays typical frequencies of operation and typical clock trees, even for the case of a square waveform, the signal that reaches the leaves of the clock line no longer has a sharp transition point and approaches the slope exhibited by the triangular signal.

This paper is organized as follows. In the next section, we discuss clock distribution and the problems associated with using a square waveform for the clock signal. In Section 3, we argue about the merits of using a triangular waveform for global clock distribution. In Section 4, voltage discretization is proposed to improve the integrity of triangular signals. Simulation results obtained on real clock lines are presented in Section 5. Section 6 concludes the paper with a summary of the arguments presented and directions for future work.

2. Issues in Clock Signal Distribution

Given the importance of the clock signal in VLSI circuits and the problems raised by the increasing clock frequency, a significant amount of research work has been put into developing methodologies for the optimization of clock distribution [5]. In this section, we analyze the most significant concerns related to this process.

2.1 Clock Skew

In a typical synchronous design, the clock signal spreads to most of the chip. Even if VLSI circuits are just

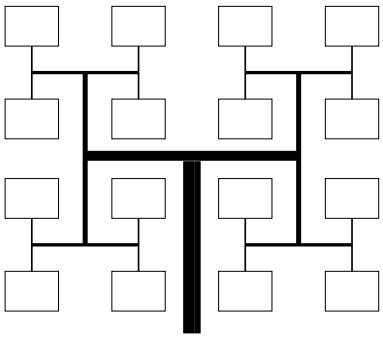

Fig. 1. H-shaped clock distribution strategy.

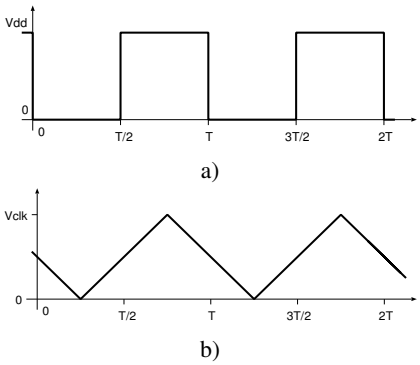

Fig. 2. a) Square waveform clock signal. b) Triangular waveform clock signal.

a few millimeters wide, with todays clock frequencies, in the order of a few GHz, tiny differences in the path from the clock generator to the different modules lead to different arrival times. This may account for a significant fraction of the clock period. The problem of the clock signal arriving at slightly different instants to different points in the circuit in known as *clock skew* [3]. The consequence is that an upper bound for the clock skew has to be discounted from the clock period. If care is not taken to minimize this effect, the amount of time remaining for useful computations can be severely diminished.

Typically, the clock signal is distributed to the modules in the circuit in terms of a tree, with buffers appropriately placed to regenerate the signal. Several topologies for this tree have been proposed with the aim of minimizing the difference in arrival times at any point in the circuit [5], [6]. Figure 1 depicts an H-shaped clock signal tree, a commonly used solution to minimize clock skew.

2.2 Noise and Signal Integrity

A square waveform, as shown in Figure 2-a), is generally used for the clock signal. Transitions between two clearly defined voltage levels define the time references necessary for synchronous operation. However, the abrupt transitions present in this type of waveform create the additional problem of inducing noise to the nearby signal lines [4].

The problem of signal integrity is compounded by the reduction of feature size, which brings signal lines closer together. Since the clock signal needs to reach every point in the circuit, this is a chip-wide problem. In pure digital circuits, this effect should be analyzed carefully in order to evaluate the possibility that it may cause the circuit to malfunction, either because it creates a glitch in a signal or because it increases the propagation delay of signals. However, it is in mixed-signal circuits that this issue is particularly sensitive [4]. In many cases, measures to isolate the clock signal need to be taken, sometimes with significant overhead.

An additional problem is that the clock line behaves like a low-pass filter. The frequency of the dominant pole reduces with the increase in resistance and capacitance of the clock line, as it becomes longer and more connected. This effect together with the higher clock frequencies implies that we have fewer significant harmonics reaching the leaves of the clock tree, causing a significant degradation of the clock signal.

2.3 Power Consumption

The simple fact that a circuit operates at higher frequencies leads to an increase in power dissipation, since this implies a larger number of computations per time unit. At the same time, the complexity of the circuits is increasing and, with it, so do the length of the clock line and the number of sequential elements this line is connected to. Hence, the total capacitance of the clock line, which needs to be charged and discharged once per clock period, is increasing significantly. This has led to a significant increase in the relative weight of the power consumed by the clock line. For some recent designs, it has been reported that the clock line can make for close to 70% of the total power consumption of the circuit [2].

Several techniques have been proposed to reduce this figure. One technique is to use a low-swing signal for the global clock distribution, and then, at the input to each module, regenerate locally the clock signal to the full voltage swing [7]. A different approach is to use a lower frequency signal for global clock distribution and multiply this frequency locally using PLL circuits [8].

Both these approaches maintain the square waveform for the global clock signal. This type of signal is the worst case for power consumption, because each transition causes a maximum spike of current over a resistive element. It can been shown that in order to minimize the power dissipated when charging or discharging a given line one should do exactly the opposite, *i.e.*, use a constant current. This can be achieved using a slowly varying voltage signal [9]. A contribution in this direction has been made in [10] where a sinusoidal signal was proposed, together with new sequential elements that operate directly with this waveform.

3. Triangular Clock Signal

The main contribution of this work is to argue that using a triangular waveform, as the one depicted in Figure 2-b)

for the global clock signal, instead of the typical square signal of Figure 2-a), can have a big impact in minimizing both noise and power consumption.

We note that the clock skew remains unaffected with the change of the waveform format. The reason for this is that we are considering signals that are even, *i.e.*, all even harmonics are 0. Since all odd harmonics are 0 at the beginning and half of the period, they cross the reference voltage at the same time independently of the number and amplitude of the harmonics. Clock skew can be mitigated through clock distribution topologies that minimizes the difference in arrival times at any point in the circuit [5], [6]. An example of a clock distribution line is the H-shaped clock signal tree, depicted in Figure 1. The ensuing discussion will thus center around noise and power dissipation.

3.1 Noise

The first observation is that, intrinsically, a triangular waveform is smoother than a square waveform. Hence, the amplitude of the harmonics of the triangular waveform decay much more rapidly than for the case of a square waveform. The amplitude of the harmonics for a square, s_k, and for a triangular, t_k, signal are given by:

$$s_k = \begin{cases} \frac{2V_{dd}}{k\pi}(-1)^{\frac{k-1}{2}}, & k \text{ odd} \\ 0, & k \text{ even} \end{cases} \qquad t_k = \begin{cases} \frac{2V_{dd}}{k^2\pi^2}, & k \text{ odd} \\ 0, & k \text{ even} \end{cases} \tag{1}$$

In the case of the triangular signal, the amplitude decreases quadratically and the first harmonic is already close to 10% of the amplitude of the base frequency, whereas the amplitude of the harmonics for the square signal only decrease linearly, and, up to the tenth harmonic, they are still within 10% of the amplitude of the base frequency of the clock signal. Therefore, for the same frequency, the triangular waveform clock signal will induce significantly less noise and will suffer less from signal degradation.

Naturally, if a sinusoidal waveform is used [10], then there are no harmonics at all. However, we note the amplitude of the harmonics for a triangular waveform is already very small, meaning that this is not a significant disadvantage, clearly not offsetting the 23% gain in power consumption, discussed next. Moreover, since voltage varies linearly with time, it is simple to use a lower clock frequency, as discussed in Section 4. Hence, the frequency components of the triangular waveform can be much lower than that of a sinusoidal wave, thus more desirable in terms of noise.

3.2 Power Consumption

Perhaps one of the main advantages of the triangular waveform over any other waveform is that it minimizes the power consumed in the resistive elements. The voltage varies linearly with time which, if done slowly enough, charges the circuit capacitances with a constant current. This is optimal in terms of power consumption. The square waveform lies exactly on the opposite side, where

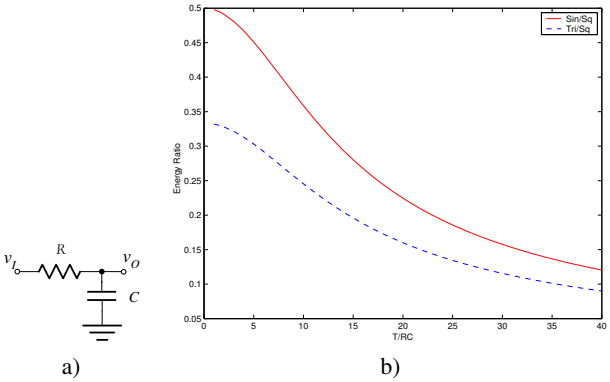

Fig. 3. Potential savings in energy per period for a single RC line as a function of T/RC: a) RC circuit; b) Plot shows the ratio of the energy consumed per clock period for triangular and sinusoidal signals over a square waveform.

the sharp transitions cause current spikes. Since power is related to the square of the current, this leads to a maximum dissipation in the resistive elements.

In Figure 3-b), we plot the potential savings in energy per period for a single RC line (see Figure 3-a)) as a function of T/RC, where T is the input signal frequency. The two curves shown refer to the ratios of the energy consumed per clock period for triangular and sinusoidal signals over a square waveform. From the picture we can see that there are indeed significant advantages for using triangular waveforms, both versus square as well as sinusoidal waveforms. For typical values of T/RC, the triangular waveform can lead to a reduction of as much as 80% in consumed power over the standard square waveform.

Note that, for normal operation, T is typically larger than RC, thus the square waveform will always present significantly larger power consumption. In this case, the energy consumed per clock period for triangular, square and sinusoidal signals, with amplitude V_{clk}, period T and driving a clock line with capacitance C is given by:

$$\begin{array}{lll} \text{Square} & \text{Sinusoidal} & \text{Triangular} \\ E_{sq} = CV_{clk}^2 & E_{sin} = \frac{\pi^2}{2}\frac{RC}{T}CV_{clk}^2 & E_{tri} = 4\frac{RC}{T}CV_{clk}^2 \end{array} \tag{2}$$

Under these conditions, the sinusoidal signal always consumes 23% more power than the triangular signal. These approximate expressions are not valid for low values of T/RC. The exact expressions for the simple RC circuit of Figure 3-a) are given in the appendix.

3.3 Waveform Generation Circuits

New sequential elements can be designed to work directly with a triangular waveform [10]. However, since that approach implies a significant shift from current designs, in this paper we simply suggest using the triangular waveform for the global clock signal, from which a regular square waveform can be generated locally at the input of each module.

Hence, we require two different circuits: (a) a square-to-triangular wave converter, to be used as the global clock

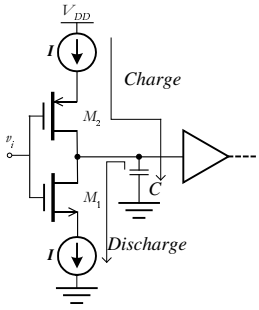

Fig. 4. Charge pump circuit for square to triangular waveform generation.

generator circuit, and (b) triangular-to-square wave converters to be used locally at the input of each module [11]. The input circuit should be able to provide a triangular waveform, and the local clock re-generator circuits should be able to provide rail-to-rail square waves Also, these circuits should be synchronous with the reference clock (external) and should be as simple as possible to minimize the overhead, both in terms of area and power consumption.

To obtain a synchronous triangular clock signal from an input reference clock we need a circuit that acts as an integrator. The most common integrator is the Miller integrator which is an inverting amplifier where the feedback component is a capacitor. For currently used clock frequencies the amplifier would be difficult to design. Another technique is to use a complete PLL (Phase Lock Loop), but this is again a complex block with high consumption and its use would depend on the need to multiply the clock frequency internally. Another way to implement an integrator is to use the input square clock to control two switches in order to charge or discharge a capacitor. This circuit is similar to a charge pump circuit (represented in Figure 4), which exhibits a small input capacitance (only two transistor gates), may operate at a frequency close to the technology limits and its power consumption depends on the clock rate and load capacitance.

To regenerate the clock locally for each digital block we will require solely a comparator, which can even consist of a simple inverter (or inverter chain).

We should point out that these circuits should not be seen as an overhead of the proposed clock distribution scheme. Even for the common square wave clock, clock buffering is required at the input and to locally perform the clock regeneration. In fact, the penalty of having a square waveform instead of triangular one may cause the comparison to be more favorable for the triangular case.

4. Reducing the Clock Frequency

Although the clock signal generator may be designed to generate a specific waveform, the signal that reaches the different modules in the circuit does not necessarily maintain these characteristics as it will be distorted by the

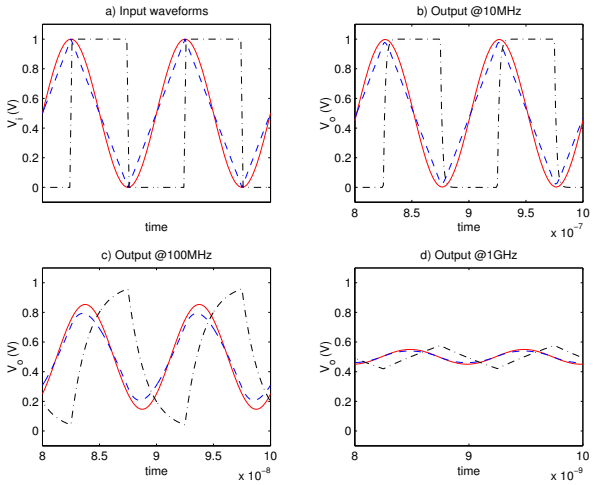

Fig. 5. Shape of the signals after an RC circuit with a pole frequency of 100MHz: a) input waveforms; b) output at 10MHz; c) output at 100MHz; d) output at 1GHz.

clock distribution line. The clock line behaves basically as a low-pass filter. Longer clock distribution trees translate to higher equivalent resistance and capacitance, thus lowering the pass band of this filter. This means that, at clock frequencies close to the dominant pole of the clock line, the clock signal soon becomes a simple sinusoid no matter the waveform format that is injected. Clock frequencies much higher than this pole lead to significant signal attenuation, which may imply a large number of signal regeneration circuitry.

We describe an experiment where the RC circuit of Figure 3-a) is used as a first approximation of a clock distribution line and it is designed to have a pole at 100MHz (R=100Ω and C= 15.9pF). It is well known that this simple RC circuit has a single pole, that, at the pole frequency, the amplitude is attenuated -3dB and that it falls at -20dB/dec after the pole. We applied at the input a square, a sinusoidal and a triangular signals, each with three different frequencies, namely 10MHz, 100MHz and 1GHz. The waveforms at the input and output (*i.e.*, at the leaves of the clock line), for the three frequencies, are presented in Figure 5.

Observing this figure we confirm that, if the pole is higher than the input frequency, the circuit does not strongly affect the input signal. However, if the pole is of the same order as the input frequency, it is already clear that the triangular and square waveforms are strongly affected by the attenuation of the higher harmonics contents of these waveforms. In this case, the output signals are closer to a sinusoid with the frequency of its fundamental component. Finally, when the input frequency is much higher than the pole, all three types of signals considered are strongly attenuated and their shape tends to a low amplitude sinusoid.

Hence, a simple analysis assuming that the triangular waveform maintains its shape throughout the clock signal

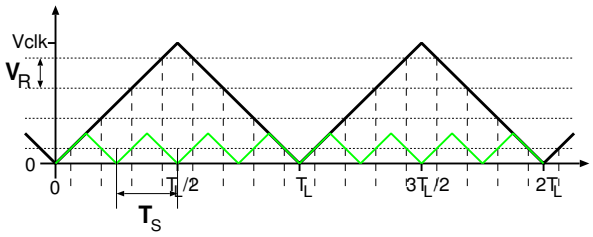

Fig. 6. An equal voltage difference translates to an equal time period.

line for all frequencies is not valid. Most likely, the power consumption will converge to the value corresponding to that of a sinusoidal signal. On the other hand, clock frequencies much higher than the pole of the clock line are not viable since the attenuation will be significant. In this case, a large number of signal regeneration circuitry may be required.

A possible solution is to reduce the frequency of the global clock signal while keeping a high frequency local clock signal. To achieve this, we make the observation that several time-slots can be easily defined in a single period of the triangular waveform, allowing for a much lower frequency for the clock signal and leading to a significant reduction in both noise and signal degradation.

In a triangular waveform, voltage varies linearly with time. Hence, we can have equidistant voltage levels define equidistant time references, as depicted in Figure 6. In this figure, voltage levels separated by $V_R = \frac{1}{4}V_{clk}$ define four time-slots of constant length T_S per period T_L of the triangular waveform. Thus, if T_S is the desired period of operation, the triangular clock signal can use a period, T_L, 4 times larger. By reducing the ratio T/RC, the lower attenuation for all signal harmonics may lead for the triangular shape to be maintained throughout the clock line, thus circumventing the problems raised above.

An equally important observation is that, according to (2), the energy consumption of a triangular wave with nV_{dd} and nT is the same for different values of n, using the proposed discretization scheme of n time slots.

Depending on the application, the voltage step V_R can be used to trade-off noise margin with global clock frequency, $T_L = \frac{V_{clk}}{V_R} \times T_S$.

In order to permit larger reductions for the frequency of the triangular waveform, its amplitude V_{clk} should be as large as possible. In todays CMOS technology, V_{clk} will be limited somewhere between 3V to 5V. One alternative that allows larger values of V_{clk} is to resort to a different technology, such as Bi-CMOS, for the circuit elements connected to the clock line. Of course, the impact on fabrication costs needs to be weighted.

5. Experimental Results

In a real clock tree circuit we do not have a simple RC circuit. Moreover, we do not even know if the capacitance at the output nodes is higher than the parasitic capacitance of long signal lines. In this section, we present results for two different circuits: first for an artificial H-shaped clock circuit with plausible characteristics, and second for a real clock tree from a commercial DSP.

TABLE I

CLOCK POWER CONSUMPTION FOR H-SHAPED AND DSP CLOCK TREES.

Clk Tree	Freq.	Square	Sinusoid		Triangular	
H Shaped	10MHz	371	11	3%	8	2%
	100MHz	4190	973	23%	657	16%
	400MHz	15179	7094	47%	5082	33%
DSP	10MHz	110	30	27%	19	17%
	40MHz	395	176	45%	123	31%

5.1 H-Shaped Clock Tree

We have considered the H-shaped clock tree circuit of Figure 1 with 16 output nodes. The circuit was extracted using a $20\mu\mathrm{m}$ length resolution for a circuit with overall size of $2 \times 2\mathrm{mm}^2$. The minimum width used in the clock tree is $2\mu\mathrm{m}$ (at the final branches near the leaves). The parameters for the resistance and capacitance were $80\mathrm{m}\Omega/\square$ and $0.03\mathrm{fF}/\mu\mathrm{m}^2$, respectively, and correspond to typical values of a $0.35\mu\mathrm{m}$ CMOS technology.

We have considered three different input frequencies, 10MHz, 100MHz and 400MHz. The power estimates in μW obtained with Spice are presented in Table I.

Although for a generic distributed RC network it is not possible to refer to a single pole, nor can we claim for this example that there is a dominant pole, we have evaluated at what frequency the transfer characteristic exhibits a -3dB gain and found this frequency to be 350MHz. For the input frequencies 10MHz and 100MHz, both below 350MHz, we observe that the triangular waveform consumes about 70% the power of a sinusoidal waveform. The savings are much larger when the comparison is made with the squared waveform. As for the results with 400MHz, the comparison between the power consumption results is no longer fair since the attenuation of the clock signal is such that we have a very attenuated and distorted clock signal reaching the leaves of the clock tree.

5.2 DSP Clock Tree

We have also considered a commercial DSP Clock Tree circuit. This clock tree has a netlist with 24334 resistances and 23282 capacitances, it has 24337 nodes and 4832 output nodes. For this example we have considered two input frequencies: 10MHz and 40MHz. The results are also shown in Table I.

In this example we do not even have a regular structure, all the paths to the output nodes are different. However, to provide some insight to the results, we have determined by simulation at what frequency the transfer characteristic exhibits a -3dB gain for a subset of the outputs. The frequencies obtained range from 22MHz to 255MHz. All these values are higher than the input frequency for the 10MHz case and the power savings in using the triangular and sinusoidal signals are in the order of what is expected.

TABLE II

COMPARISON OF THE POWER CONSUMPTION OF TWO TRIANGULAR SIGNALS, ONE USING V_{dd}, T AND THE OTHER $4V_{dd}, 4T$.

Clk Tree	Freq.	V_{dd}, T	$4V_{dd}, 4T$	
H Shaped	10MHz	8	8	100%
	100MHz	657	829	126%
	400MHz	5082	10880	214%
DSP	10MHz	19	24	126%
	40MHz	123	321	261%

For the 40MHz input clock frequency, we see that the relation between the triangular and sinusoidal and the traditional square wave degrades as expected. As for the relation between the triangular and sinusoidal clock signals we can see it remains approximately 70% for both cases and that the small reduction in the relation is in part not an advantage because is due to a lower amplitude of the triangular signal after filtering when comparing to the sinusoidal one.

5.3 Results using Voltage Discretization

In order to explore the observations made in Section 4, we have also analyzed for the triangular waveform clock signal the case where both the period and the amplitude is multiplied by 4. The results are presented in Table II.

We can observe that the power consumption of the two cases of the triangular waveforms is similar when the clock frequency is below the frequency of the dominant pole. For higher clock frequencies (400MHz in the case of the H-shaped clock network and 40MHz for the DSP), the $4V_{dd}, 4T$ triangular waveform consumes more the twice the power of the V_{dd}, T one. This comparison is, again, not fair and misleading since, for these two cases, the V_{dd}, T waveform is very attenuated, hence the lower power consumption. On the other hand, because of its lower frequency, the $4V_{dd}, 4T$ waveform maintains its shape, meaning that it will require fewer circuits for signal regeneration.

6. Conclusions

We have presented arguments that show that a triangular clock signal is advantageous in terms of noise, signal degradation and power consumption.

The results we present were obtained without considering any signal regeneration circuitry. It is clear that for the DSP clock tree case, higher operating frequencies would require clock regeneration for any input waveform. The impact of the triangular signal would be even higher if signal regeneration circuitry is used, since the frequency at the -3dB point can be reduced significantly, allowing for lower triangular signal frequencies.

We have also made the observation that the linearity of this signal allows for simple voltage discretization. This, in turn, permits a lower frequency of operation for the triangular signal, from which a higher operation rate can be extracted locally.

Future work includes analyzing the efficiency of the circuits to generate a triangular waveform and to extract a square wave from a triangular one. In parallel, we plan to develop sequential circuits that can operate directly on a triangular waveform.

Acknowledgments

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Appendix

The following expressions indicate the exact expression for the energy consumed per clock period in a series RC circuit of Figure 3-a) ($RC = \tau$). Expressions were derived assuming square, E_{sq}, sinusoidal, E_{sin}, and triangular, E_{tri}, waveforms, of period T, amplitude V_{dd} and DC value $V_{dd}/2$.

$$E_{sq} = \frac{1-e^{-T/\tau}}{\left(1+e^{-T/2\tau}\right)^2} CV_{dd}^2$$
$$E_{sin} = \frac{\pi^2}{2}\frac{\tau}{T}\frac{1}{1+(2\pi\frac{\tau}{T})^2} CV_{dd}^2$$
$$E_{tri} = 2\frac{\tau}{T}CV_{dd}^2\left(1 + 16\frac{\tau}{T}\frac{e^{-T/2\tau}-1}{1+e^{-T/2\tau}} + 8\frac{\tau}{T}\frac{1-e^{-T/\tau}}{(1+e^{-T/2\tau})^2}\right) \quad (3)$$

It is easy to show that with $T >> RC$ these expression lead to those in (2) in Section 3.

References

[1] G. Martin and H. Chang, "System-on-Chip Design," in *Proceedings of the 4th International Conference on ASICs*, 2001, pp. 12–17.

[2] C. Anderson *et al.*, "Physical Design of a Fourth-Generation POWER GHz Microprocessor," in *Proceedings of the IEEE International Solid-State Circuits Conference*, 2001, pp. 232–233.

[3] H. Sutoh *et al.*, "Circuit Technique for Skew-Free Clock Distribution," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, 1995.

[4] E. Albuquerque and M. Silva, "Evaluation of Substrate Noise in CMOS and Low-Noise Logic Cells," in *Proceedings of the International Symposium on Circuits and Systems*, vol. 4, May 2001, pp. 750–753.

[5] E. Friedman, "Clock Distribution Networks in Synchronous Digital Integrated Circuits," *Proceedings of the IEEE*, vol. 89, no. 5, pp. 665–692, May 2001.

[6] P. Restle and A. Deutsch, "Designing the Best Clock Distribution Network," in *Symposium on VLSI Circuits - Dig. Tec.*, 1998, pp. 2–5.

[7] M. Igarashi *et al.*, "A Low-Power Design Method using Multiple Supply Voltages," in *Proceedings of the IEEE Symposium on Low Power Electronics*, August 1997, pp. 36–41.

[8] T. Olsson, P. Nilsson, T. Meincke, A. Hemani, and M. Torkelson, "A Digitally Controlled On-Chip Clock Multiplier for Globally Asynchronous Locally Synchronous Systems," in *Proceedings of the Midwest Symposium on Circuits and Systems*, 1999.

[9] C. Seitz, A. Frey, S. Mattisson, S. Rabin, D. Speck, and J. Snepscheut, "Hot-Clock nMOS," in *Proceedings of the 1985 Chapel-Hill Conference on VLSI*, 1985, pp. 1–17.

[10] B. Voss and M. Glesner, "A Low Power Sinusoidal Clock," in *Proceedings of the International Symposium on Circuits and Systems*, vol. 4, May 2001, pp. 108–111.

[11] H.-H. Chang, I.-H. Hua, and S.-I. Liu, "A Spread-Spectrum Clock Generator with Triangular Modulation," *IEEE J. Solid-State Circ.*, vol. 38, pp. 673–676, April 2003.