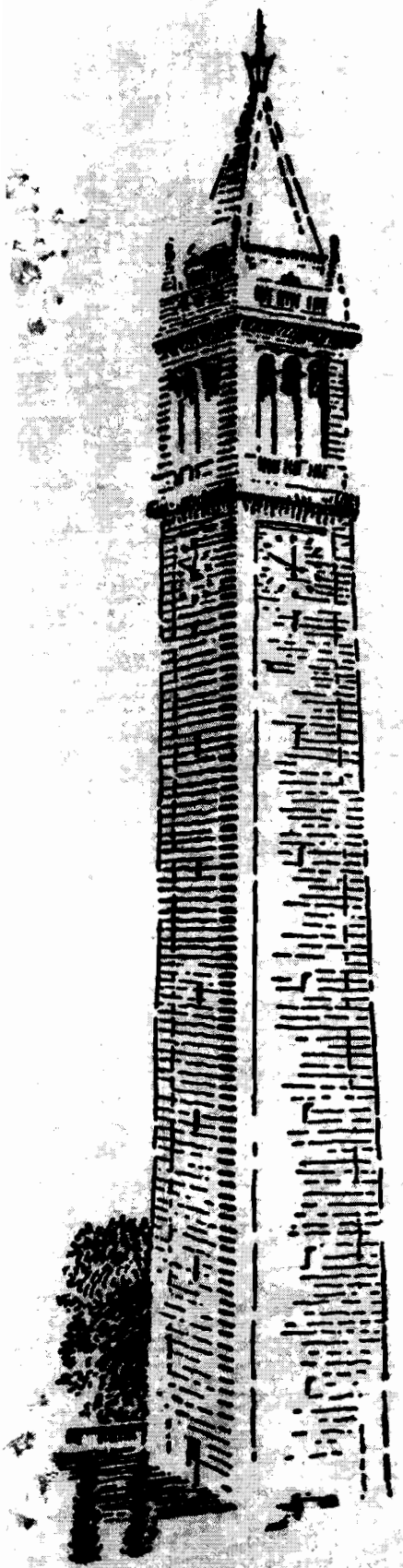

SPICE

(Simulation Program with Integrated Circuit Emphasis)

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Simulation Program with Integrated Circuit Emphasis (SPICE)

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Abstract

A new circuit simulation program, SPICE, is described. The simulation capabilities of nonlinear dc analysis, small signal analysis, and nonlinear transient analysis are combined in a nodal analysis program to yield a reasonably general purpose electronic circuit simulation program. Particular emphasis is placed upon the circuit models for the BJT and the FET which are implemented in SPICE.

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I. Introduction

The use of a digital computer to simulate the electrical characteristics of electronic circuits has been an important part of circuit design and evaluation since the advent of integrated circuits. The peculiarities of integrated circuit design, such as the need for dc coupling and minimal use of resistances, made hand analysis of even the earliest analog integrated circuits impractical. Increased size and complexity of both analog and digital integrated circuits have made computer simulation an even more important factor in efficient circuit design. A circuit simulation program has an additional advantage at academic institutions, in that it provides students with a "dry lab" capability. In essence, each student is supplied with his own "workbench" where he can design, build, and test circuits in a fraction of the time and expense that a real laboratory would require. This allows for a more relevant and educational set of assignments than normally would be possible in the time constraints of an academic term.

Because of the several advantages of computer simulation, we have been heavily involved in the development and use of simulation programs for several years. We found available programs to be either too cumbersome or too inefficient for classroom use, and it became necessary to develop our own set of simulation programs. The first program developed at our laboratory was BIAS [1]. The need for a transient analysis capability lead to the development of CANCER [2] and TIME [3]. A new version of TIME, entitled SINC, has been developed by S. P. Fan at our laboratory. Our program SLIC (Simulator for Linear Integrated Circuits) [4] was developed especially for the simulation of analog integrated circuits. The latest program developed at our laboratory is SPICE (Simulation Program with Integrated Circuit Emphasis). This program is an improvement of the CANCER program and is used extensively for classroom instruction and graduate research for the large signal simulation of analog and digital integrated circuits.

II. Description of SPICE

SPICE is a general purpose simulation program for integrated circuits. It contains the three basic analysis capabilities which provide the bulk of information of a circuit's performance: a) nonlinear dc analysis, with the provision for "stepping" an input source to obtain a set of static transfer curves, b) small-signal, sinusoidal steady-state analysis, including a noise analysis [5] to evaluate noise performance, c) nonlinear, time-domain, transient analysis. The circuit size limitations for SPICE are 400 nodes, and 200 total elements, of which no more than 100 can be semiconductor devices. A user's guide for the SPICE program is included in the Appendix.

Built-in models are included for the most common semiconductor devices: diodes, bipolar junction transistors (BJT's), junction field-effect transistors (JFET's), and metal-oxide-semiconductor field-effect transistors (MOSFET's). The BJT models are based on either the Ebers-Moll [10] or the Gummel-Poon [17] formulations; the models for the FET's are derived from the model of Shichman and Hodges [6].

Because SPICE is used extensively for undergraduate instruction, it was designed to be easy to learn and easy to use. The input language is free format to minimize user errors. Where possible, the program supplies "default" values for circuit parameters that are not specified,

so that the beginning user need specify only a few model parameters and program control parameters to effect a simulation. Simulation results are available either as tabular listings of the output variables or as line printer plots. The program contains 8000 Fortran IV statements, and requires 40,000 decimal words of core memory to execute on the CDC 6400 available at the University of California, Berkeley. *

The basic program organization is shown in Figure 1. The circuit is described on a set of punched cards. The program first reads and processes the input deck and checks for input errors. The next step in the simulation is establishing the necessary set of pointers for the sparse matrix routines [7]. These pointers enable the two dimensional Y matrix to be collapsed into a one dimensional vector containing only the nonzero Y-matrix terms. The matrix routines then operate only on the nonzero terms contained in this vector. This saves a substantial amount of core memory and central processor execution time.

The next step in the simulation is the actual analysis. One set of routines is used for the iterative solution of the nodal equations for dc analysis or for a given timepoint in the transient analysis [2], and another set of routines is used for the solution of the complex nodal equations in the small signal analysis.

The final simulation step is the output phase, where the appropriate tabular listings and line printer plots are generated.

As mentioned earlier, SPICE is an improvement of the CANCER program, and many of the algorithms used in SPICE are the same as those used in CANCER and discussed in Ref. [2]. In particular, the sparse matrix routines in both CANCER and SPICE are improvements of those originally developed by Berry [7]. The basic Newton iteration algorithm of SPICE and CANCER are the same, and both programs use an implicit, trapezoidal integration formula and a fixed, user supplied timestep for transient analysis. The small-signal routines are similar, except that a representation of flicker ($\frac{1}{f}$) noise [8] has been added to the noise analysis of SPICE. The actual Fortran coding has been substantially improved in the transition from CANCER to SPICE.

III. BJT Models

The most significant development in SPICE is the implementation of adequate device models for the BJT, JFET, and MOSFET. Because the BJT is so important in integrated circuits, the BJT model deserves special attention.

Two BJT models were necessary to accomodate the separate needs for a simple model to be used in classroom use and for a more sophisticated model for graduate research. Both models are represented by the electrical schematic shown in Figure 2. The charge storage elements Q_{BE} and Q_{BC} [9] represent the stored base charge and depletion layer charges. The parasitic elements r_c, r_b, r_e, and C_{CS} are assumed to be constant. The dc characteristics of the simpler model are derived from the familiar Ebers-Moll model [10] with an added representation of basewidth modulation [11]. The dc, intrinsic model is defined by the terminal equations:

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*An overlaid version can be executed in approximately 25,000 decimal words.

$$I_C = I_S\left[\exp\left(\frac{qV_{BE}}{kT}\right) - \exp\left(\frac{qV_{BC}}{kT}\right)\right]\left[1 - \frac{V_{BC}}{V_A}\right] - \frac{I_S}{\beta_r}\left[\exp\left(\frac{qV_{BC}}{kT}\right) - 1\right]$$

$$I_B = \frac{I_S}{\beta_f}\left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right] + \frac{I_S}{\beta_r}\left[\exp\left(\frac{qV_{BC}}{kT}\right) - 1\right]$$

where q is the electronic charge, k is Boltzman's constant, and T is the absolute temperature. The remaining variables, I_S, β_f, β_r, and V_A, are user supplied model parameters. The saturation current, I_S, is the extrapolated intercept current of log (I_C) versus V_{BE} in the forward region and log (I_E) versus V_{BC} in the reverse region as shown in Figure 3. The parameters β_f and β_r are the forward and reverse short circuit current gains, respectively, which are assumed not to vary with operationg point. The parameter V_A, referred to as the "Early voltage", produces a finite value of output conductance, g_o, due to basewidth modulation. The output conductance is given by the equation:

$$g_o \equiv \frac{\partial I_C}{\partial V_{CE}} = \frac{I_S}{V_A}\left[\exp\left(\frac{qV_{BE}}{kT}\right) - \exp\left(\frac{qV_{BC}}{kT}\right)\right] + \frac{qI_S}{kT}\exp\left(\frac{qV_{BC}}{kT}\right)\left[1 - \frac{V_{BC}}{V_A}\right] \simeq \frac{I_C}{V_A}$$

Hence, output conductance is proportional to I_C, with the constant of proportionality being $(\frac{I}{V_A})$. A graphical intepretation of V_A is shown in Figure 4.

The nonlinear charge storage elements Q_{BE} and Q_{BC} are determined by the equations:

$$Q_{BE} = \tau_F I_S\left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right] + C_{jeo}\int_o^{V_{BE}}\left[1 - \frac{V}{\phi_e}\right]^{-m_e} dV$$

$$Q_{BC} = \tau_R I_S\left[\exp\left(\frac{qV_{BC}}{kT}\right) - 1\right] + C_{jco}\int_o^{V_{BC}}\left[1 - \frac{V}{\phi_c}\right]^{-m_c} dV$$

Possibly a more meaningful method of expressing these charge storage element equations is the voltage dependent, small-signal capacitance formulae:

$$C_{BE} = \frac{\partial Q_{BE}}{\partial V_{BE}} = \tau_F\left(\frac{qI_S}{kT}\right)\exp\left(\frac{qV_{BE}}{kT}\right) + C_{jeo}\left[1 - \frac{V_{BE}}{\phi_e}\right]^{-m_e}$$

$$C_{BC} = \frac{\partial Q_{BC}}{\partial V_{BC}} = \tau_R\left(\frac{qI_S}{kT}\right)\exp\left(\frac{qV_{BC}}{kT}\right) + C_{jco}\left[1 - \frac{V_{BC}}{\phi_c}\right]^{-m_c}$$

Charge storage is modeled by two base storage terms, which are characterized by the transit times τ_f and τ_r, and two depletion terms which are characterized by the parameters C_{jeo}, ϕ_e, and m_e for the emitter depletion region and C_{jco}, ϕ_c, and m_c for the collector depletion region. For the simple Ebers-Moll model, the parameters m_e and m_c are fixed at a value of 0.5. The numerical instability of the depletion layer capacitance formulae is avoided by using a linear approximation for depletion capacitance in forward bias.

The simpler Ebers-Moll transistor model lacks a representation of many of the important second order effects present in actual devices; the two most important neglected effects are high level injection, which causes a drop in β_f and β_r and an increase in τ_f and τ_r when high level injection is reached [12, 13, 14], and depletion layer recombination, which causes a drop in τ_f and τ_r at low levels of collector current [15]. These effects are included in the more complicated BJT model that is implemented in SPICE. This model is an adaptation of the model proposed by Gummel and Poon [16, 17, 18]. The equations for the dc characteristics are:

$$I_C = \frac{I_S}{Q_B}\left[\exp\left(\frac{qV_{BE}}{kT}\right) - \exp\left(\frac{qV_{BC}}{kT}\right)\right] - \frac{I_S}{\beta_{RM}}\left[\exp\left(\frac{qV_{BC}}{kT}\right) - 1\right] - C_4 I_S\left[\exp\left(\frac{qV_{BC}}{n_c kT}\right) - 1\right]$$

$$I_B = \frac{I_S}{\beta_{FM}}\left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right] + C_2 I_S\left[\exp\left(\frac{qV_{BE}}{n_e kT}\right) - 1\right]$$

$$+ \frac{I_S}{\beta_{RM}}\left[\exp\left(\frac{qV_{BC}}{kT}\right) - 1\right] + C_4 I_S\left[\exp\left(\frac{qV_{BC}}{n_c kT}\right) - 1\right]$$

where the normalized base charge, Q_B, is defined by the equations:

$$Q_1 = 1 + \frac{V_{BC}}{V_A} + \frac{V_{BE}}{V_B}$$

$$Q_2 = \frac{I_S}{I_k}\left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right] + \frac{I_S}{I_{kr}}\left[\exp\left(\frac{qV_{BC}}{kT}\right) - 1\right]$$

$$Q_B = \frac{1}{2}\left[Q_1 + \sqrt{Q_1^2 + 4Q_2}\right]$$

The model parameters for the dc portion of the Gummel-Poon model are I_S, β_{fm}, β_{rm}, C_2, C_4, n_e, n_c, I_k, I_{kr}, V_A, and V_B. The charge storage elements Q_{BE} and Q_{BC} are identical to the SPICE Ebers-Moll model.

The second order effect of depletion layer recombination is included in the model with the two nonideal base current components determined by the parameters C_2 and n_e for the emitter depletion region and C_4 and n_c for the collector region. This is shown in the graph of I_B against V_{BE} shown in Figure 5. Both the effect of basewidth modulation and a simple treatment of high level injection are introduced into the model via the base charge term, Q_B. This is best understood by considering two limiting cases. First, consider the case when $Q_2 \approx 0$. Then, in the forward region,

$$I_C \approx \frac{I_S}{1 + \frac{V_{BC}}{V_A} + \frac{V_{BE}}{V_B}} \exp\left(\frac{qV_{BE}}{kT}\right) \approx I_S \exp\left(\frac{qV_{BE}}{kT}\right)\left[1 - \frac{V_{BC}}{V_A}\right].$$

Hence, the parameter has the same interpretation, for small values of V_{BC}, as it does for the simpler SPICE model. A similar argument holds for the reverse Early voltage, V_B, in the reverse region.

Now consider the case when $Q_1 \approx 1$. Then, in the forward region, with low level injection,

$$\frac{4I_S}{I_k} \exp\left(\frac{qV_{BE}}{kT}\right) << 1,$$

the collector current follows the "ideal" law:

$$I_C \approx I_S \exp\left(\frac{qV_{BE}}{kT}\right).$$

For high levels of injection,

$$\frac{4I_S}{I_k} \exp\left(\frac{qV_{BE}}{kT}\right) >> 1,$$

the collector current becomes "nonideal".

$$I_C \approx \sqrt{\frac{I_k}{I_S}} \exp\left(\frac{qV_{BE}}{2kT}\right).$$

Hence, the emission coefficient changes from 1 (ideal) to 2 as predicted by first order theory [12]. A similar argument holds for the reverse region, where high level injection occurs when

$$\frac{4I_S}{I_{kr}} \exp\left(\frac{qV_{BC}}{kT}\right) >> 1.$$

The parameters I_k and I_{kr} are termed the forward knee current and the reverse knee current, and can be interpreted as the approximate value of collector current (for forward region) and emitter current (for reverse region) where high level injection becomes significant.

Perhaps more insight into the SPICE Gummel-Poon parameters is obtained by inspection of the asymptotic behavior of the short circuit current gain as shown in Figure 6. The current gain is essentially constant at a value of β_{FM} for collector currents greater than I_L, falls off with a slope of $1 - 1/n_e$ for collector currents less than I_L, and falls off with a slope of -1 for collector currents greater than I_k; I_L, the low current breakpoint, is given by the equation:

$$I_L = I_S \left[C_2 \beta_{FM}\right]^{\frac{n_e}{n_e - 1}}$$

This, of course, is only an asymptotic relation. For cases where low level and high level effects overlap, as is true in most transistors, some trial and error is required to obtain the correct parameters.

Although not obvious from the defining equations, the effective transit times of the device, and hence the f_T is also dependent upon collector current. The effective forward transit time is given by:

$$\tau_f[e_{ff}] = \frac{Q_{BE}}{I_C} \cong \tau_f Q_B$$

Hence, as high level injection is reached, τ_f is no longer constant but instead is directly proportional to Q_B, as shown in Figure 7.

The more complex Gummel-Poon model that is implemented in SPICE has been quite adequate for the graduate research in our laboratory [19]. However, we anticipate the necessity of adding current dependent base resistance [12] and base pushout [17] into the model.

Default and typical values for the Ebers Moll and Gummel-Poon models parameters are given in the Appendix.

IV. Circuit examples

The shunt-series feedback amplifier shown in Figure 8 provides an illustrative example of the difference between the two BJT models in an actual circuit simulation. This circuit was simulated using the model parameters shown in Table 1. The graph of the forward current gain against I_C is superimposed on the asymptotic curve shown in Figure 6. For the Ebers-Moll model, β_F was chosen to match the amplifier gain in the Gummel-Poon simulation. The first stage of the circuit operates at a bias current one decade above the lower knee current, I_l = 1 μA while the second stage is biased at 1 mA. The upper knee current I_k is 3 mA. Since the circuit is current-driven, the effects of a current-dependent beta are more pronounced than with a voltage-driven circuit.

The dc transfer curve of V_{out} against I_{in}, for the open loop case (R_{F1} and R_{F2} removed), is shown in Figure 9. The maximum dc swing predicted by the two models differs by 48%, while the small signal gain at zero input differs by about 12%. In the transient analysis, a 0.02 μA (peak-to-peak) sine wave with a frequency of 100kHz was applied to the input. The Ebers-Moll simulation predicted an output voltage of 2.00 volts (peak-to-peak), while the Gummel-Poon simulation predicted an output voltage of 1.78 volts (peak-to-peak).

When the simulation was repeated for the closed loop case (R_{F1} and R_{F2} are now included; the loop gain is 2.65) the maximum dc swing was of course the same; the small-signal gain differed by about 6% for the two models, and the transient output voltage differed by about 7% for the two models.

The necessity for a more complex BJT model is obviously circuit dependent. The above example was purposefully chosen to accentuate the differences between the two models; in many circuit designs the difference in the predicted waveforms is much less. The central processor time required for these two simulations was 4.6 sec for the Ebers-Moll model and 5.2 sec for the Gummel-Poon model. Of these times, 2.1 sec was required for reading, error checking, matrix setup, and output; the Gummel-Poon model hence requires 25% additional time on a per Newton iteration basis or 13% total additional job time.

Additional simulation execution times are shown in Table 2 for a SN7400 TTL inverter and in Table 3 for the μA 741 operational amplifier. Both of these examples used the Ebers-Moll transistor model. These times were observed on the CDC 6400 computer available at the University of California Computer Center at Berkeley.

V. FET Models

The increasing use of the MOSFET device in digital integrated circuits, and to a lesser extent the JFET device in analog integrated circuits, necessitated the inclusion of suitable models for these two devices. The circuit schematic for the JFET model used in SPICE is shown in Figure 10.

The two parasitic ohmic resistances, r_d and r_s, are assumed to be constant. The equation for internal drain current, I_D, is taken as a simple square-law relation with an added parameter to model channel width modulation [6]. The piecewise relations for the various regions of operation of the JFET are:

I. $V_{DS} > 0$ (forward region)

$$I_D = \begin{cases} 0 & V_{GS} - V_{TO} < 0 \\ \beta(V_{GS} - V_{TO})^2 (1 + \lambda V_{DS}) & 0 < V_{GS} - V_{TO} < V_{DS} \\ \beta V_{DS}[2(V_{GS} - V_{TO}) - V_{DS}] (1 + \lambda V_{DS}) & 0 < V_{DS} < V_{GS} - V_{TO} \end{cases}$$

II. $V_{DS} < 0$ (reverse region)

$$I_D = \begin{cases} 0 & V_{GD} - V_{TO} < 0 \\ -\beta(V_{GD} - V_{TO})^2 (1 - \lambda V_{DS}) & 0 < V_{GD} - V_{TO} < -V_{DS} \\ \beta V_{DS}[2(V_{GD} - V_{TO}) + V_{DS}] (1 - \lambda V_{DS}) & 0 < -V_{DS} < V_{GD} - V_{TO} \end{cases}$$

The three dc parameters which determine the JFET operation are V_{TO}, β, and λ. The parameter V_{TO}, which is always negative for JFET's, is most commonly referred to as the "pinchoff" voltage.* The parameters β and V_{TO} are probably best understood by examining the graph of transconductance, g_m, as a function of V_{GS} (in the forward, saturated region) as shown in Figure 11. The transconductance is assumed to be a linear function of V_{GS} with a slope of 2β. The parameter λ is analogous to the parameter V_A for BJT's. The output conductance of the device, in the forward saturated region, is given by the equation:

$$g_d \text{sat} = \beta\lambda(V_{GS} - V_{TO})^2 \approx \lambda I_D$$

Hence, the output conductance is assumed to vary linearly with drain current, with the constant of proportionality being λ. The graphic interpretation of the parameter is shown in Figure 12.

The two gate junctions are modeled as ideal diodes with the following defining equations:

$$I_{GS} = I_S\left[\exp\left(\frac{qV_{GS}}{kT}\right) - 1\right]$$

$$I_{GD} = I_S\left[\exp\left(\frac{qV_{GD}}{kT}\right) - 1\right]$$

The charge storage elements, Q_{GS} and Q_{GD}, are modeled as ideal, step junction depletion capacitances. Because the gate junctions are normally reverse biased, the diffusion charge storage mechanism is omitted. The charge storage elements are defined by the equations:

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*V_{TO} is assumed to be negative for all depletion mode devices irrespective of channel polarity.

$$Q_{GS} = C_{GSO} \int_0^{V_{GS}} \frac{dV}{\left(1 - \frac{V}{\phi_\beta}\right)^{1/2}}$$

$$Q_{GD} = C_{GDO} \int_0^{V_{GD}} \frac{dV}{\left(1 - \frac{V}{\phi_\beta}\right)^{1/2}}$$

As for the depletion capacitances in the bipolar models, these charge storage elements can also be expressed in terms of the voltage dependent, small signal capacitances:

$$C_{GS} = C_{GSO}\left[1 - \frac{V_{GS}}{\phi_\beta}\right]^{-1/2}$$

$$C_{GD} = C_{GDO}\left[1 - \frac{V_{GD}}{\phi_\beta}\right]^{-1/2}$$

The MOSFET model used in SPICE is very similar to the model proposed by Shichman and Hodges.[6] Although more sophisticated models for the MOSFET device have been proposed,[23,24], we have found this model adequate for our investigations. It includes a representation of the effect of substrate bias on gate threshold voltage and a representation of the effect of channel width modulation. The circuit schematic for the SPICE MOSFET model is shown in Figure 13. The internal drain current generator, I_D, is given by the following piecewise equations for all regions of operation of the MOSFET device:

I. $V_{DS} > 0$ (forward region)

$$V_{TE} = V_{TO} + \gamma\left[\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right]$$

$$I_D = \begin{cases} 0 & V_{GS} - V_{TE} < 0 \\ \beta(V_{GS} - V_{TE})^2 (1 + \lambda V_{DS}) & 0 < V_{GS} - V_{TE} < V_{DS} \\ \beta V_{DS}[2(V_{GS} - V_{TE}) - V_{DS}] (1 + \lambda V_{DS}) & 0 < V_{DS} < V_{GS} - V_{TE} \end{cases}$$

II. $V_{DS} < 0$ (reversed region)

$$V_{TE} = V_{TO} + \gamma\left[\sqrt{\phi - V_{BD}} - \sqrt{\phi}\right]$$

$$I_D = \begin{cases} 0 & V_{GD} - V_{TE} < 0 \\ -\beta(V_{GD} - V_{TE})^2 (1 - \lambda V_{DS}) & 0 < V_{GD} - V_{TE} < -V_{DS} \\ \beta V_{DS}[2(V_{GD} - V_{TE}) + V_{DS}] (1 - \lambda V_{DS}) & 0 < -V_{DS} < V_{GD} - V_{TE} \end{cases}$$

The five dc parameters which determine the operating characteristics of the MOSFET are: V_{TO}, β, λ, γ and ϕ. The interpretation of the parameters V_{TO}, β and λ is similar to the interpretation of these parameters for the JFET. In the case of the MOSFET, V_{TO} is positive for an enhancement mode device (the usual case) and negative for a depletion mode device. The actual threshold voltage of the device depends on the substrate bias, as shown in the graph of V_{TE} against V_{BS} in Figure 14. The parameters γ and ϕ determine the actual shape of this curve. The parameter V_{TO} is the zero substrate bias value of threshold voltage.

The two substrate (bulk) junctions are modeled by ideal diodes with the following defining equations:

$$I_{BS} = I_S \left[\exp\left(\frac{qV_{BS}}{kT}\right) - 1 \right]$$

$$I_{BD} = I_S \left[\exp\left(\frac{qV_{BD}}{kT}\right) - 1 \right]$$

The charge storage effects in the MOSFET device are modeled by five capacitances. The capacitors C_{GD}, C_{GS}, and C_{GB} are assumed to be constant. The charge storage elements Q_{BD} and Q_{BS} are treated as ideal, step junction depletion capacitances. Since the substrate junctions are normally reverse biased, the diffusion charge storage mechanism is omitted. These two charge storage elements are defined by the equations:

$$Q_{BD} = C_{BDO} \int_0^{V_{BD}} \frac{dV}{[1 - \frac{V}{\phi_B}]^{1/2}}$$

$$Q_{BS} = C_{BSO} \int_0^{V_{BS}} \frac{dV}{[1 - \frac{V}{\phi_B}]^{1/2}}$$

These elements can also be expressed in terms of the voltage dependent, small signal capacitances:

$$C_{BD} = C_{BDO} \left[1 - \frac{V_{BD}}{\phi_B}\right]^{-1/2}$$

$$C_{BS} = C_{BSO} \left[1 - \frac{V_{BS}}{\phi_B}\right]^{-1/2}$$

We have found these FET models quite adequate for both instructional use and research. To attain reasonable convergence in the dc analysis it is necessary to limit the change in V_{GS} and V_{GD} from iteration to iteration, just as it is necessary to limit junction voltage changes.[2] We have found an acceptable limit to be $0.1 + |V_{TO}|$ (volts). The gate junctions for JFET's and the substrate junctions for MOSFET's are modeled by an equivalent conductance

$$g_{eq} = \frac{q\, I_S}{kT}$$

in the reverse bias region (where they normally operate). With these precautions, we have found the convergence properties of the FET models to be comparable to those of the BJT models.

Default and typical values for JFET and MOSFET model parameters are shown in the Appendix.

VI. Conclusions

The implementation of suitable device models for the BJT and FET's, coupled with improved program coding and organization, has provided us with a simulation program which is much more powerful and efficient than its predecessor, CANCER. However, one can never assume that a simulation program is complete, and we forsee many enhancements for SPICE at the time of this writing.

The most desirable addition to the program is a reliable timestep control in the transient analysis. Our program SINC has a timestep control which is based on the iteration count at each timepoint; however, we have found this method not totally satisfactory in controlling the stability properties of the trapezoidal method. Instead, it is necessary to estimate and control the truncation error at each timepoint to obtain a satisfactory transient solution. Because of the method in which an integration algorithm is implemented in a nodal analysis program [2, 20], the use of variable order integration methods [21, 22] constitute a tremendous increase in the program code. Furthermore, our research has shown that higher order integration algorithms are poorly suited to the highly nonlinear digital logic circuits because of their inherent poor stability properties. The major problem in a timestep control is the estimation of truncation error, which amounts to numerical differentiation. Since higher order formulae require estimation of higher order derivatives, a reliable estimation of truncation error can only become more difficult as order is increased. At this time, it appears that a single order, probably Euler or Trapezoidal, is the most reliable and efficient integration algorithm to use in a nodal analysis program.

VII. Acknowledgements

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ADDENDUM

Flicker Noise Analysis in SPICE

The ability to simulate flicker noise sources in the noise analysis of SPICE (refer to IEEE Journal of Solid State Circuits, August 1971, pp. 204-215) has been added to SPICE. Flicker noise is included by adding another term to the current generators for the devices:

a. Junction diodes

$$i_D^2 = 2q\ I_D\ \Delta f + \frac{KI_D^a}{f}\ \Delta f$$

b. Bipolar Junction Transistors

$$i_B^2 = 2q\ I_B\ \Delta f + \frac{KI_B^a}{f}\ \Delta f$$

c. Field effect transistors (both JFET's and MOSFET's).

$$i_{DS}^2 = 4kT(\frac{2}{3}\ g_m)\ \Delta f + \frac{KI_D^a}{f}\ \Delta f$$

For bipolar devices, our measurements have shown that a=1 for npn devices and a=1.5 for pnp devices, and $K=6.6 \times 10^{-16}$ for npn devices and 0.3×10^{-13} for pnp devices (these measurements are for the devices in a 741 operational amplifier, but should be representative of monolithic devices in general).

Operationally, the flicker noise parameters are defined on the .MODEL card by setting two parameters:

FNK	Flicker noise coefficient	Default=0.0
FNA	Flicker noise exponent	Default=0.1

These parameter names are the same for all four devices. Hence, a model card for an npn transistor, with flicker noise, might look like:

```
.MODEL M1 NPN BF=35 RB=100 RE=0.1 IS=1.5E-15 FNK=6.6E-16 FNA=1.0
```

External Models in SPICE

The ability to define an arbitrary device which contains allowable elements has been included in SPICE (versions 1G and later). Hence the gate shown in Figure 1 could be defined to be an element in SPICE just as a bipolar device is a model in SPICE. The restrictions are:

a. External models cannot be nested, that is, an external model cannot contain an external model.

b. An external model cannot have more than 20 external nodes (the gate on the following page has 5 external nodes and three internal nodes).

To define an external model, a group of cards is required. The first card is a .MODEL card which contains the word .MODEL, the name of the model, the letter X, and the external nodes of the device. The following cards are the set of element cards which define the model card, and the last card is a .FINIS card, which contains simply the word .FINIS. The following group of cards defines the TTL gate shown in Figure 1.

```
.MODEL TTLGATE X 1 2 3 4 5
Q1 6 8 1 M1
Q2 6 8 2 M1
Q3 6 8 3 M1
Q4 4 6 7 M1
Q5 4 7 0 M1
```

```
R1 5 4 1K
R2 7 0 1.5K
R5 5 8 4K
.MODEL M1 NPN BF=80 RB=50 TF=0;1NS TR=10NS CJC=0.3PF CJE=0.5PF
.FINIS
```

Once the model has been defined, it can be referenced just as an internal built-in model is referenced. The "device" name must begin with the letter X. The device is specified by the name, the external nodes, and the model name. For example, the logic circuit shown in Figure 2 could be simulated by the following group of cards:

```
EXAMPLE LOGIC CIRCUIT
VCC 10 0 DC 5
VIN1 1 0 PULSE 0 5 10NS 10NS 10NS 100NS
VIN2 2 0 PULSE 0 5 200NS 10NS 10NS 100NS
XG1  1 1 1 3 10 TTLGATE
XG2  1 1 2 4 10 TTLGATE
XG5  5 2 4 5 10 TTLGATE
.OUT V5 5 0 PLOT TRAN
.TRAN 5NS 500NS
.MODEL TTLGATE X 1 2 3 4 5
Q1 6 8 1 M1
Q2 6 8 2 M1
Q3 6 8 3 M1
Q4 4 6 7 M1
Q5 4 7 0 M1
R1 5 4 1K
R2 7 0 1.5K
R3 5 8 4K
.MODEL M1 NPN BF=80 RB=50 TF=0.1NS TR=10NS CJC=0.3PF CJE=0.5PF
.FINIS
.END
```

DC Sensitivity Analysis in SPICE

A dc sensitivity analysis capability was also included in SPICE (versions IG and later) but never documented. This option is used to obtain the dc, small-signal sensitivities of a given output variable with respect to every circuit value. The general format for sensitivity analysis is:

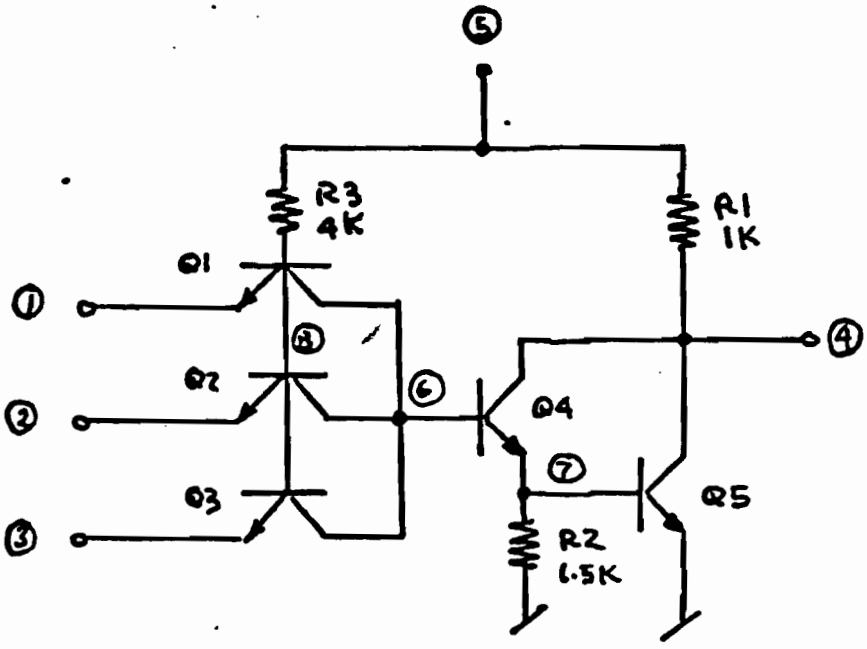
```
.SENS     ovar 1     ovar 2     ...     ovar 10
```

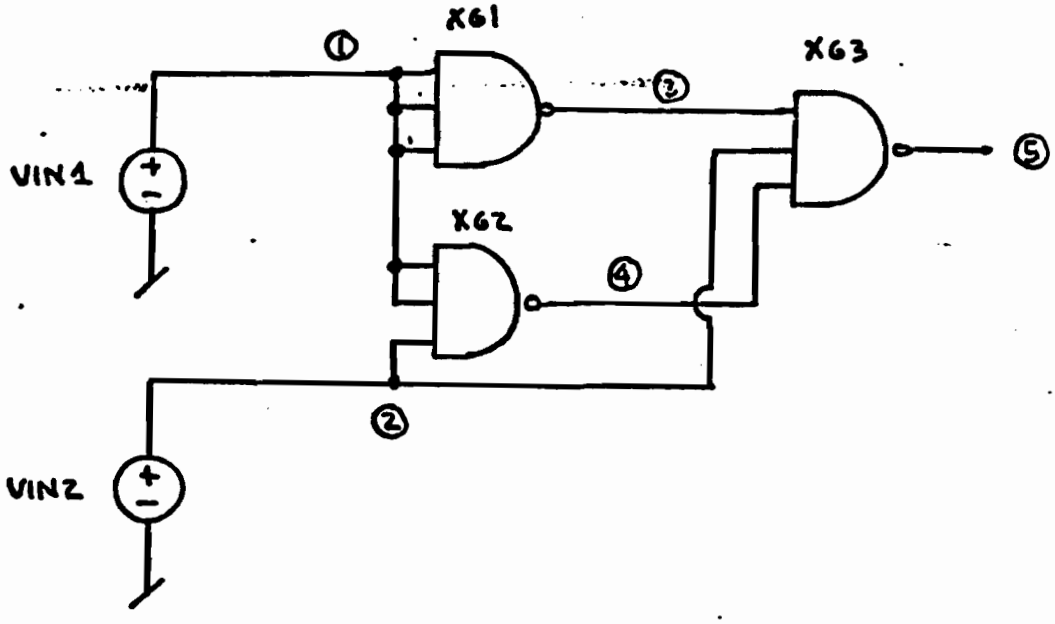
Note that from one to ten outputs can be specified. Only one .SENS card should be used in a deck. The syntax for the output variables (ovar 1 ... ovar n) is identical to the syntax for output variables in the .OUTPUT card.

Examples:

```
.SENS VOUT 3 2
.SENS V1 1 0 V2 2 0 IX VCC
```

If a .SENS card is included in the SPICE data deck, the program will compute the dc, small-signal sensitivities (derivatives) at each specified output variable with respect to every circuit value (including the dc parameters for BJT model and diode model). There is no way of selecting specific sensitivities. In the first example, the program will compute and print the derivative of the voltage between node 3 and node 2 with respect to every circuit parameter.


5
R3
4K
R1
1K
Q1
1
8
Q2
2
6
Q4
4
7
Q3
3
Q5
R2
1.5K


X61
1
X63
3
5
VIN1
X62
4
2
VIN2

SPICE 1Q (1 Mar 74)

The latest version of SPICE, SPICE 1Q, is now released. Versions 1M, 1N, 1O, and 1P were all local versions, so 1Q is the replacement version for SPICE 1L. In contains the following modifications:

1. Overlay organization - The program structure has been modified slightly to readily accomodate an overlay structure. The program requires a 60000 octal region to execute on the CDC 6400 computer at the University of California, Berkeley.

2. Distortion analysis - A new analysis algorithm for computing the small-signal distortion performance of a linear circuit has been implemented. For further details on the theory of distortion analysis, see Trans. IEEE, Vol. CT-7, November 1973, pp. 709 - 717 and pp. 742 - 746.

3. Revised .OUTPUT control card - To accomodate distortion analysis; and to add some flexibility to the AC analysis output, the .OUTPUT format has been modified.

4. Assembly language matrix routines - The matrix decomposition and solution routines have been recoded in COMPASS assembly language. For CDC users, this results in a savings of 10% - 40%. For non-CDC users, the FORTRAN code has been included, as comments, in the assembly routines, and can be easily reinstated.

5. Addition of the .RUN card - The .RUN control card has been added to allow the printing of various execution statistics (matrix structure, number of iterations, and timing data for each phase of a simulation).

6. FET convergence - The routines for JFET's and MOSFET's have been modified to improve the convergence of simulations involving JFET's and MOSFET's.

7. Small-signal dc transfer curve errors - An error in the computation of the dc, small-signal input resistance, transfer function, and output resistance has been corrected.

8. Gummel-Poon temperature dependence - An error that caused the saturation currents in the Gummel-Poon transistor model to be computed incorrectly (as a function of temperature) has been corrected.

9. Voltage source polarity error - An error that caused the polarity of voltage sources to sometimes be reversed has been corrected.

SPICE 1Q INPUT FORMAT CHANGES

1. Distortion analysis

SPICE will compute the distortion characteristics of the circuit in a small-signal mode as a part of the ac small-signal sinusoidal steady-state analysis if requested. The analysis is performed assuming that signals of two frequencies are imposed at the input; let the two frequencies be f_1 and f_2.

The program then computes the following distortion measures:

HD2 - The magnitude of the frequency component 2 f_1 assuming that f_2 is not present.

HD3 - The magnitude of the frequency component 3 f_1 assuming that f_2 is not present.

SIM2 - The magnitude of the frequency component $f_1 + f_2$

DIM2 - The magnitude of the frequency component $f_1 - f_2$

DIM3 - The magnitude of the frequency component $2f_1 - f_2$

All of these distortion measures can be computed at each frequency point (value of f_1) and printed or plotted (either as REAL and IMAG, or as MAG, DB, and PHASE) just as any other output variable. In addition, at specified frequencies, the contribution of every nonlinear device to the total distortion can be printed.

Distortion analysis is specified on the .AC card:

```
.AC DEC 10 1 10KHZ DISTO RLOAD INTER REFPWR SKW2 SPW2
   -------------          ---------------------
   any legal freq         optional - defaults
   variation format       supplied if not specified
```

WHERE:

RLOAD - The name of the output load resistor into which all distortion power products are to be computed (must be specified).

INTER - The interval at which the summary printout of the contributions of all nonlinear devices to the total distortion is to be printed. Zero implies no printout, 1 implies every point, 2 implies every other point, 3 implies every third point, and so on. Defaults to zero if not specified.

REFPWR - The reference power level used in computing the distortion products. If not specified, a value of 1 mW (that is, dBm) is used.

SKW2 - The ratio of f_2 to f_1. If not specified, a value of 0.9 is used (i.e., $f_2 = 0.9\ f_1$).

SPW2 - The amplitude of f_2. A value of 1.0 is used if not specified.

EXAMPLE: .AC DEC 10 1.0 100K DISTO RL 2 1.0E-3 0.95 0.75

2. Output options (.OUTPUT card)

Some new options have been added to the .OUTPUT card to accomodate distortion analysis and improve output for AC analysis:

.OUTPUT	Vxxxxxx N1 N2 Ixxxxxx Vyyyyy	.PRINT (options)	.PLOT (options)
	ONOISE	either print or plot or both can	
	RINOISE	be deleted	
	HD2		
	HD3		
	SIM2		
	DIM2		
	SIM3		

The output variable Vxxxxxx is a voltage output (N1 is the positive node, and N2 is the negative node), Ixxxxxx is a current output (Vyyyyyy is the voltage source the current is flowing in), ONOISE is the output noise computed in the noise analysis, RINOISE is the reflected input noise computed in the noise analysis, and HD2, HD3, SIM2, DIM2, and DIM3 are the distortion measures mentioned in distortion analysis.

The options available are:

DC	dc analysis output
TR	transient analysis output
MAG	ac analysis output, magnitude
DB	ac analysis output, magnitude (in dB)
PHS	ac analysis output, phase
RE	ac analysis output, real part
IM	ac analysis output, imaginary part

Some output examples:

To plot a transient response of node voltage 4

```
.OUTPUT V4 4 0 PLOT TR
```

To print and plot the dc transfer curve for node voltage 17 and the bode plot for node voltage 17

```
.OUTPUT V17 17 0 PRINT DC MAG DB PHS PLOT MAG DB PHS DC
```

To plot the output noise and equivalent input noise in both volts and dB:

```
.OUTPUT ONOISE PLOT MAG DB
.OUTPUT RINOISE PLOT MAG DB
```

To plot the distortion measures HD2, HD3, DIM2, and DIM3:

```
.OUTPUT HD2 PLOT DB PHS
.OUTPUT HD3 PLOT DB PHS
.OUTPUT DIM2 PLOT DB PHS
.OUTPUT DIM3 PLOT DB PHS
```

3. .RUN card - If a .RUN card is included in the input deck, the program will print matrix statistics, circuit statistics, and timing information. This data is not printed if the .RUN card is absent.

MUTUAL INDUCTORS

SPICE 1Q also contains provision for specifying a coupling between inductors in the circuit. A mutual inductance is specified by the following card:

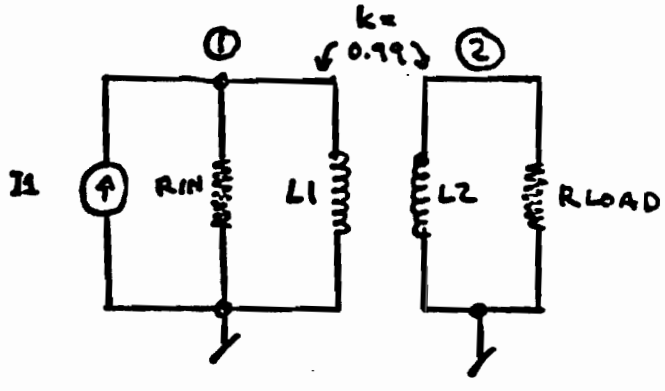
Uxxxxxx Lyyyyyy Lzzzzzz value

The name must begin with a U. Lyyyyyy and Lzzzzzz are the two coupled inductors, and 'value' is the value of mutual inductance between the inductors. The coefficient of coupling, k, is defined by:

$$k = \frac{M}{L_1 L_2}$$

where M is the mutual inductance, and L_1 and L_2 are the values of inductance for the two coupled inductors. This coefficient of coupling must always be less than unity in absolute value. A negative value of M inverts the direction in which current flows. The following data deck defines an ac analysis of the simple transformer circuit shown below.

```
TEST OF MUTUAL INDUCTANCE
I1 0 1 AC 1
RIN 1 0 1K
L1 1 0 1UH
L2 2 0 1UH
U12 L1 L2 0.99UH
RLOAD 2 0 1K
.AC DEC 10 10  100KHZ
.OUTPUT V1 1 0 PLOT MAG PHS
.OUTPUT V2 2 0 PLOT MAG PHS
.END
```



TYPICAL BJT AND FET PARAMETERS

For bipolar transistors, forward and inverse current gains, output conductance or Early voltage, and emitter saturation current are measured at a typical active region operating point. Collector series resistance is measured at a typical saturated region operating point. Base series resistance is calculated from mask dimensions and base sheet resistance. The three depletion layer capacitances are calculated at zero bias from mask dimensions and process specifications. Forward and inverse transit times are calculated from these capacitances (under bias) and measured values of forward and inverse current gain-bandwidth (f_T), taken at a typical operating point. These eleven paramenters are adequate to characterize integrated circuit bipolar transistors in almost all analog and digital applications. Representative values for a small IC transistor are given in Table I.

Once these parameters are known for one transistor made by a given process, parameters for devices of differing mask geometry may be determined without further measurements. Current gains, Early voltage, and transit times are to first order independent of mask geometry for npn IC transistors. Emitter saturation current, junction capacitances, and series resistances are simple functions of mask dimensions and process specifications. The most troublesome parameters in this scaling process are the inverse current gain and inverse transit time; due to the trend toward non-saturating and Schottky clamped circuits, the significance of these parameters is decreasing. In such circuits, inverse parameters have virtually no influence on circuit performance.

This approach to modeling bipolar IC components usually will produce circuit simulation results accurate to within .05 V in DC levels and to within 10% in time and frequency domain characteristics. Substantially more effort is needed to reduce errors by a factor of two.

A similar approach works well for MOS transistor model parameter determination. A sample device made by the chosen process is evaluated. Threshold voltage, gain factor (k or Beta), body effect coefficient, and output conductance or Early voltage are measured. The five inter-electrode capacitances are calculated from mask dimensions and process specifications. Source-body and drain-body capacitances are those of normal pn junctions. Gate area and oxide capacitance determine the total capacitance from gate to source, body, and drain. This capacitance may be divided into two or three parts. For static MOS circuits, dividing this capacitance into equal, constant gate-source and gate-drain components is simple and adequate. For dynamic circuits (particularly the ratioless type), gate capacitance should be divided into three voltage-dependent parts. Representative parameters for a small p-channel silicon-gate MOS transistor are shown in Table II.

Parameters for other MOS transistors, differing in mask geometry from the sample device, are obtained by scaling. Gain factor and capacitances are simple functions of geometry; the other parameters are independent of geometry in first-order approximation.

FORWARD BETA	100
INVERSE BETA	5
EMITTER SATURATION CURRENT	2×10^{-16} A
EARLY VOLTAGE	50 V
COLLECTOR SERIES RESISTANCE	50 Ω
BASE SERIES RESISTANCE	50 Ω
FORWARD TRANSIT TIME	0.3 nS
INVERSE TRANSIT TIME	10 nS
EMITTER JUNCTION CAPACITANCE	0.5 pF
COLLECTOR JUNCTION CAPACITANCE	0.5 pF
SUBSTRATE JUNCTION CAPACITANCE	1.0 pF

TABLE I

CHANNEL WIDTH TO LENGTH RATIO	1.0
THRESHOLD VOLTAGE	2 V
GAIN FACTOR	2 $\mu A/V^2$
BODY EFFECT	0.75 $V^{1/2}$
EARLY VOLTAGE	50 V
SOURCE-BODY CAPACITANCE	0.05 pF
DRAIN-BODY CAPACITANCE	0.05 pF
GATE-SOURCE CAPACITANCE	0.01 pF
GATE-DRAIN CAPACITANCE	0.01 pF
GATE-BODY CAPACITANCE	0

TABLE II

REFERENCES

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[16] H. K. Gummel, "A Charge Control Relation for Bipolar Transistors," Bell System Tech. J., vol. 49, Jan. 1970, pp. 115-120.

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TABLE 1

BJT MODEL PARAMETERS FOR SHUNT-SERIES FEEDBACK AMPLIFIER

EBERS-MOLL		GUMMEL-POON	
β_F	75	β_{FM}	100
β_R	1	β_{RM}	1
I_S	1.0×10^{-14}	I_S	1×10^{-14}
r_b	0	r_b	0
r_c	0	r_c	0
r_e	0	r_e	0
τ_F	1 ns	C_2	100
τ_R	0	I_k	3mA
C_{cs}	0	n_e	2
C_{jeo}	0	C_4	0
C_{jco}	1 pF	I_{kR}	infinite
ϕ_e	1	n_c	2
ϕ_c	1	τ_F	1 ns
VA	50	τ_R	0
		C_{cs}	0
		C_{jeo}	0
		C_{jco}	1pF
		V_A	50
		V_B	infinite
		ϕ_e	1
		m_e	0.5
		ϕ_c	1
		m_c	0.5

TABLE 2

EXECUTION TIMES FOR SN7400 TTL INVERTER
(27 NODES, 8 BJT'S, 101 TIMEPOINTS)

READIN	0.42 sec
SETUP	0.08 sec
DC ANALYSIS	0.52 sec
(ITERATIONS)	(22)
TRANSIENT	7.26 sec
(ITERATIONS)	(340)
OUTPUT	0.92 sec
TOTAL	9.20 sec

TIME PER NEWTON ITERATION: 21.4 msec

TIME PER NEWTON INTERATION PER BJT: 2.7 msec

TABLE 3

EXECUTION TIMES FOR 741 OP AMP
(49 NODES, 22 BJTS, 101 TIMEPOINTS)

READIN	0.8 sec
SETUP	0.5 sec
DC ANALYSIS	0.9 sec
(ITERATIONS)	(12)
TRANSIENT	13.6 sec
(ITERATIONS)	(203)
OUTPUT	0.9 sec
TOTAL	16.7 sec

TIME PER NEWTON ITERATION:	67 msec
TIME PER NEWTON INTERATION PER BJT:	3 msec

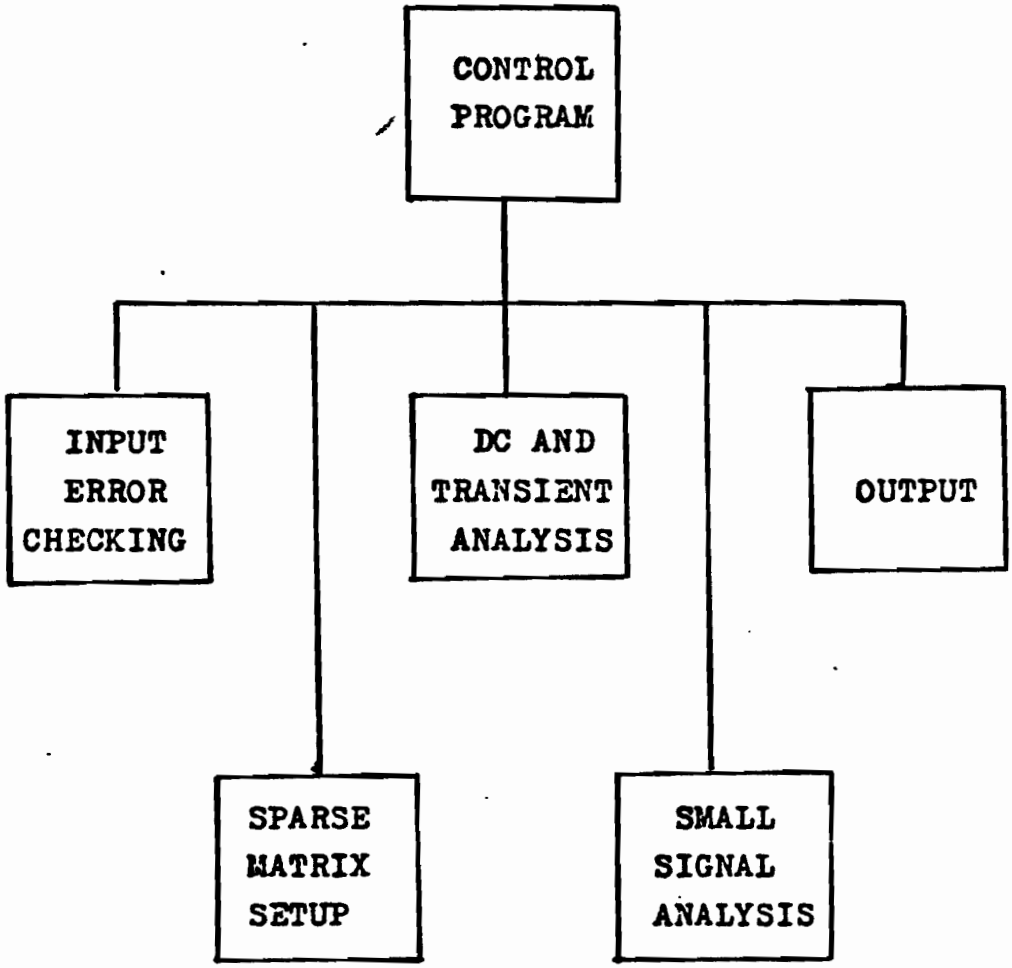

CONTROL PROGRAM
INPUT ERROR CHECKING
DC AND TRANSIENT ANALYSIS
OUTPUT
SPARSE MATRIX SETUP
SMALL SIGNAL ANALYSIS

Figure 1

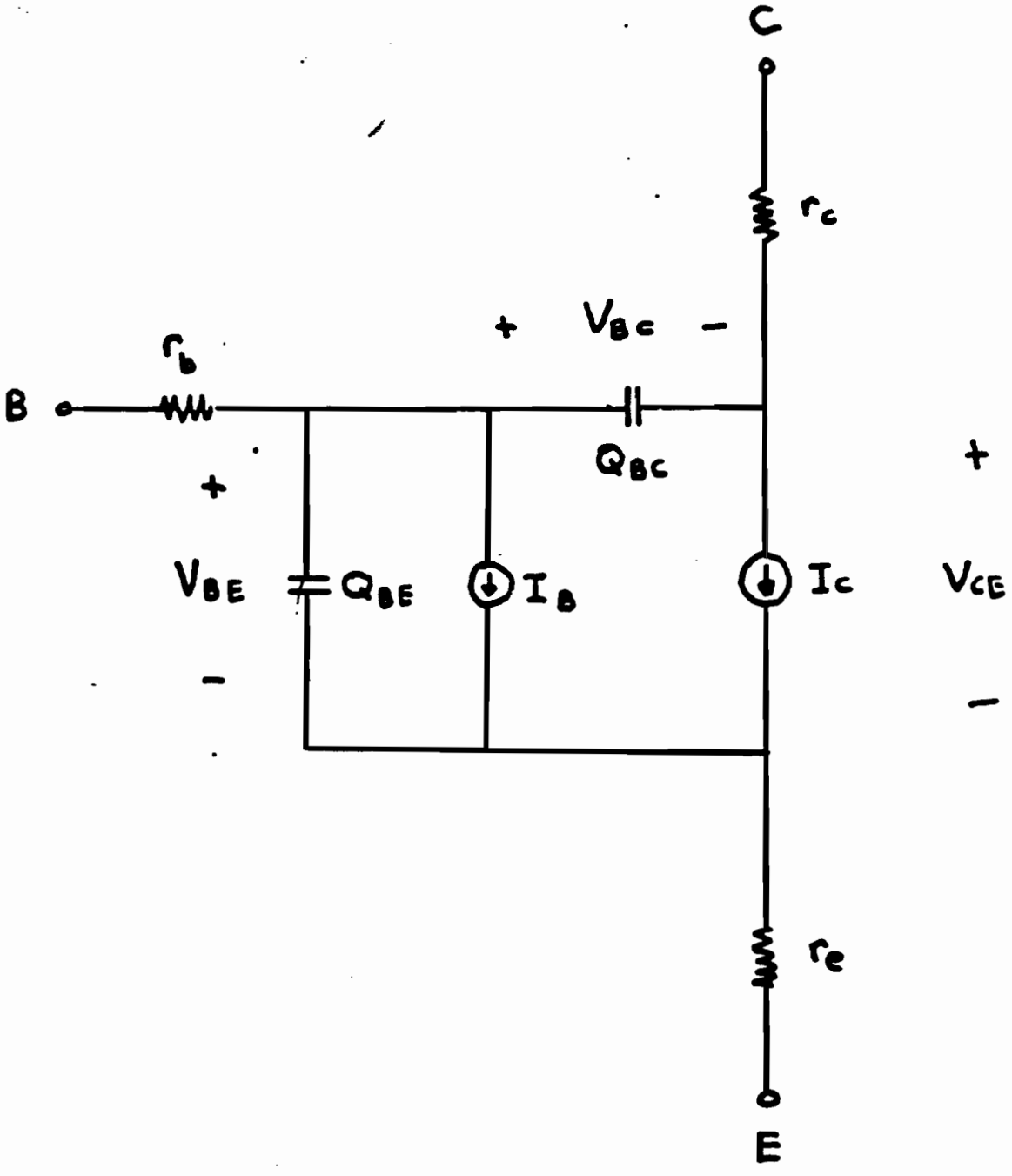


Figure 2

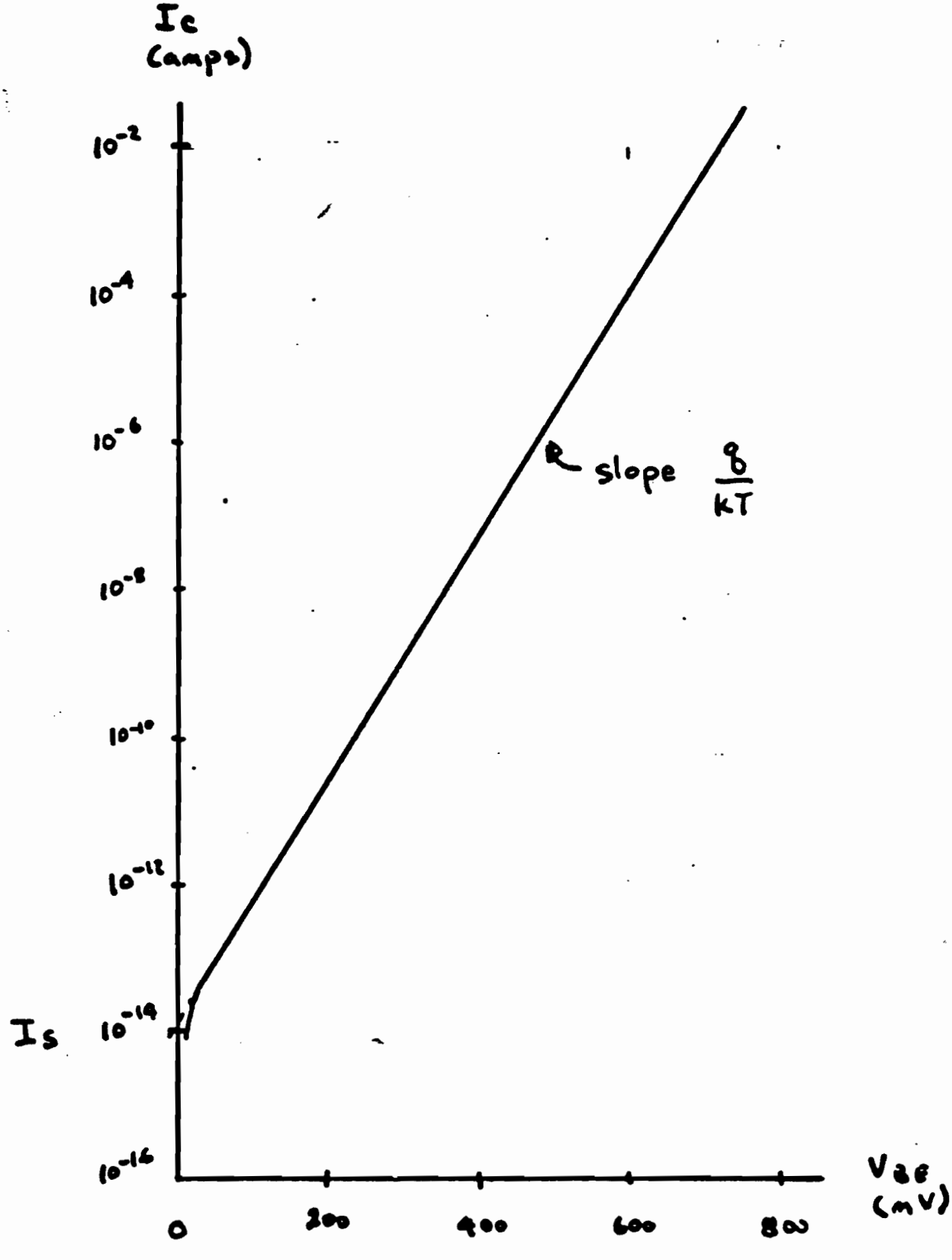

Ic
(amps)
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
10^{-14}
10^{-16}
Is
slope $\frac{q}{kT}$
0
200
400
600
800
Vbe
(mV)

Figure 3

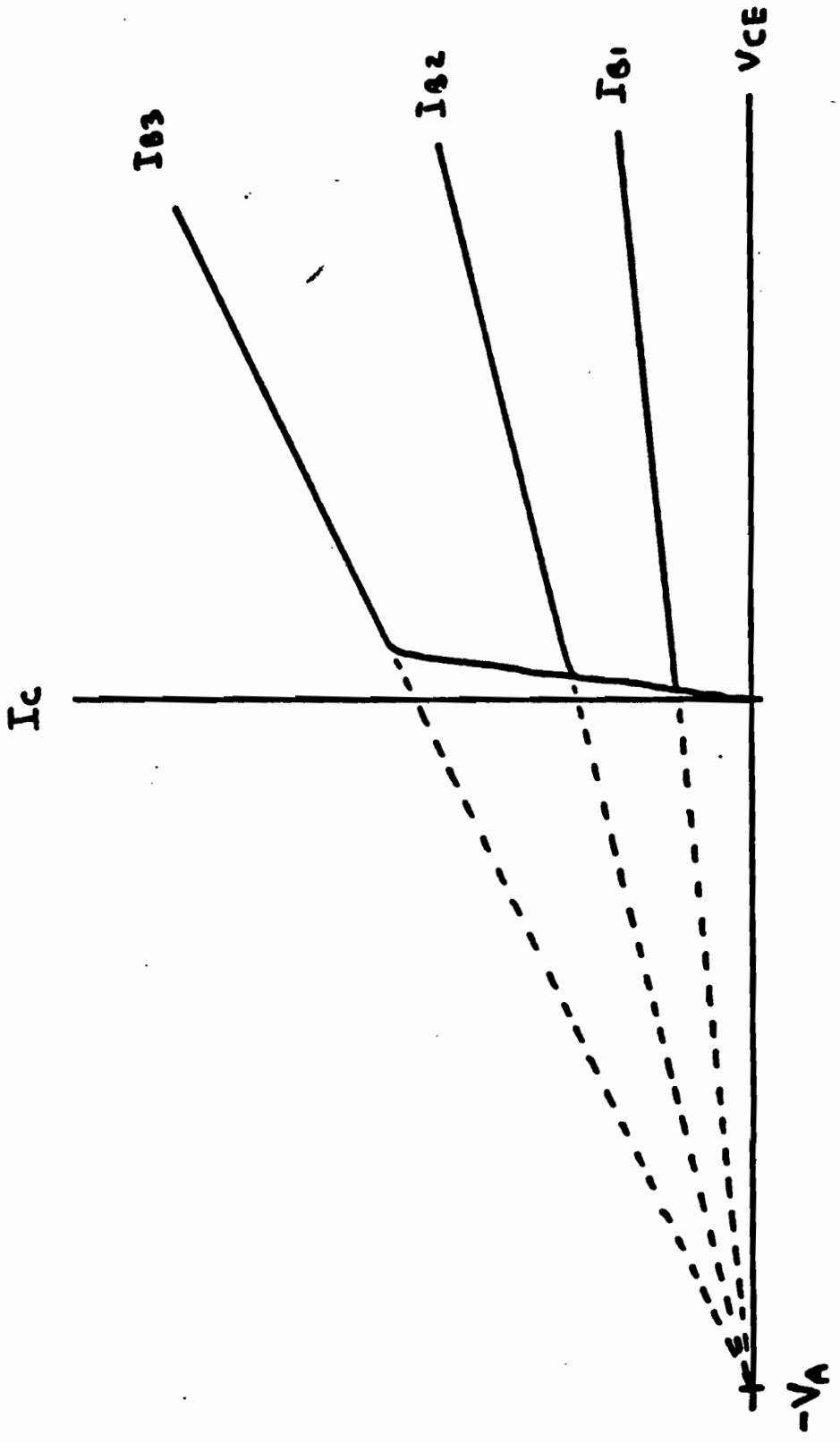


Figure 4

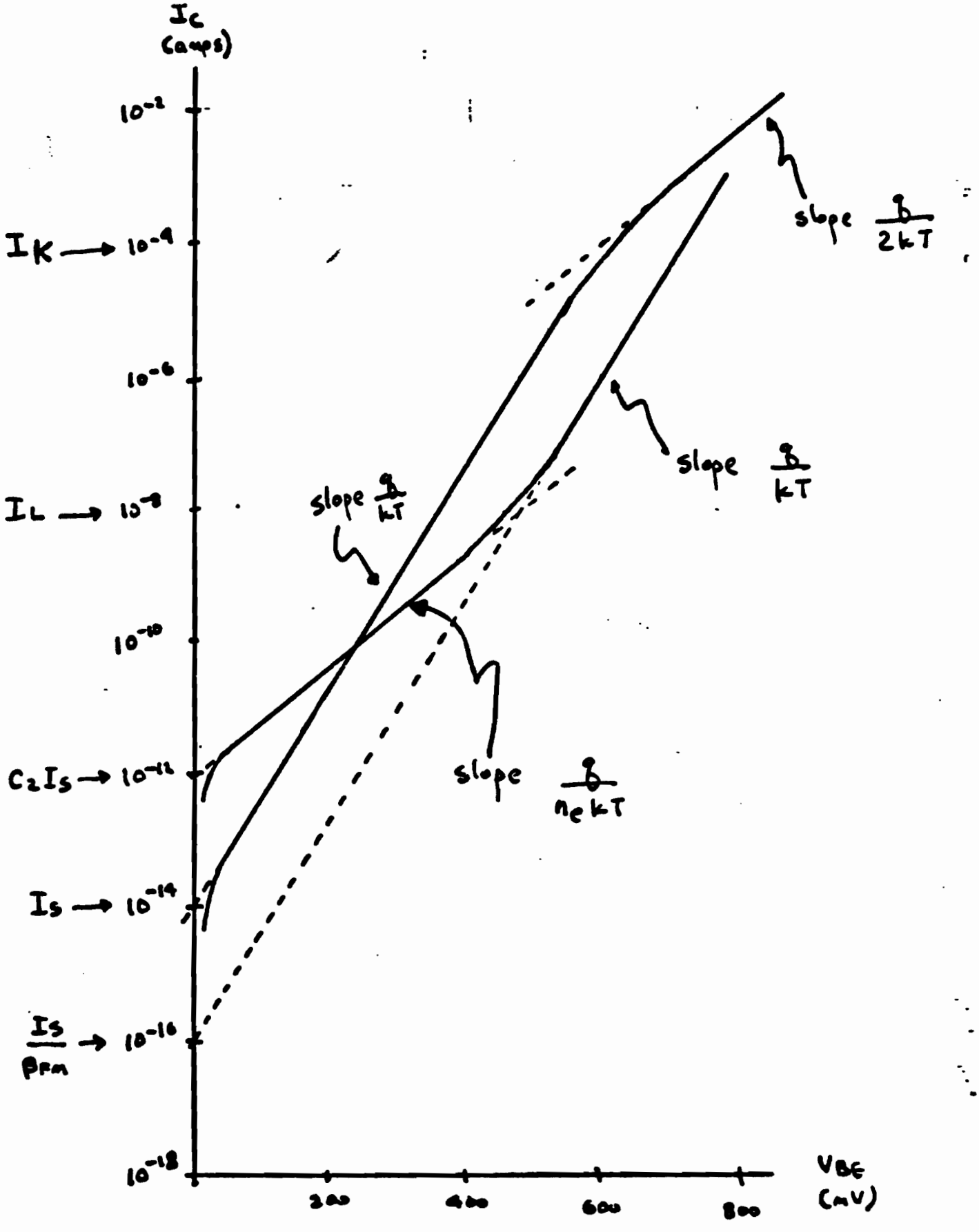

I_C (amps)
10^{-2}
$I_K \rightarrow 10^{-9}$
10^{-6}
$I_L \rightarrow 10^{-3}$
10^{-10}
$C_2 I_S \rightarrow 10^{-11}$
$I_S \rightarrow 10^{-14}$
$\frac{I_S}{\beta_{FM}} \rightarrow 10^{-16}$
10^{-18}
slope $\frac{q}{2kT}$
slope $\frac{q}{kT}$
slope $\frac{q}{kT}$
slope $\frac{q}{n_e kT}$
200
400
600
800
V_{BE} (mV)

Figure 5

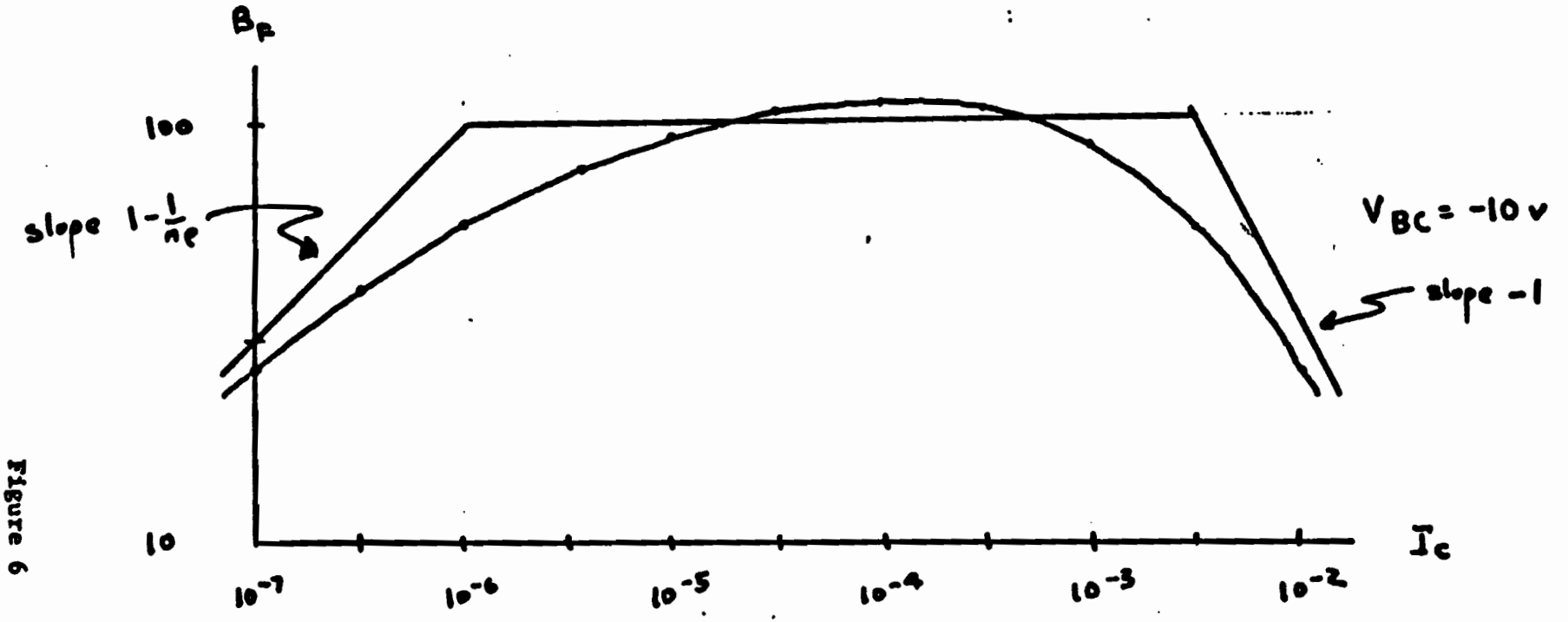


Figure 6

$I_K = 3$ mA

$C_2 = 100$

$\beta_{FM} = 100$

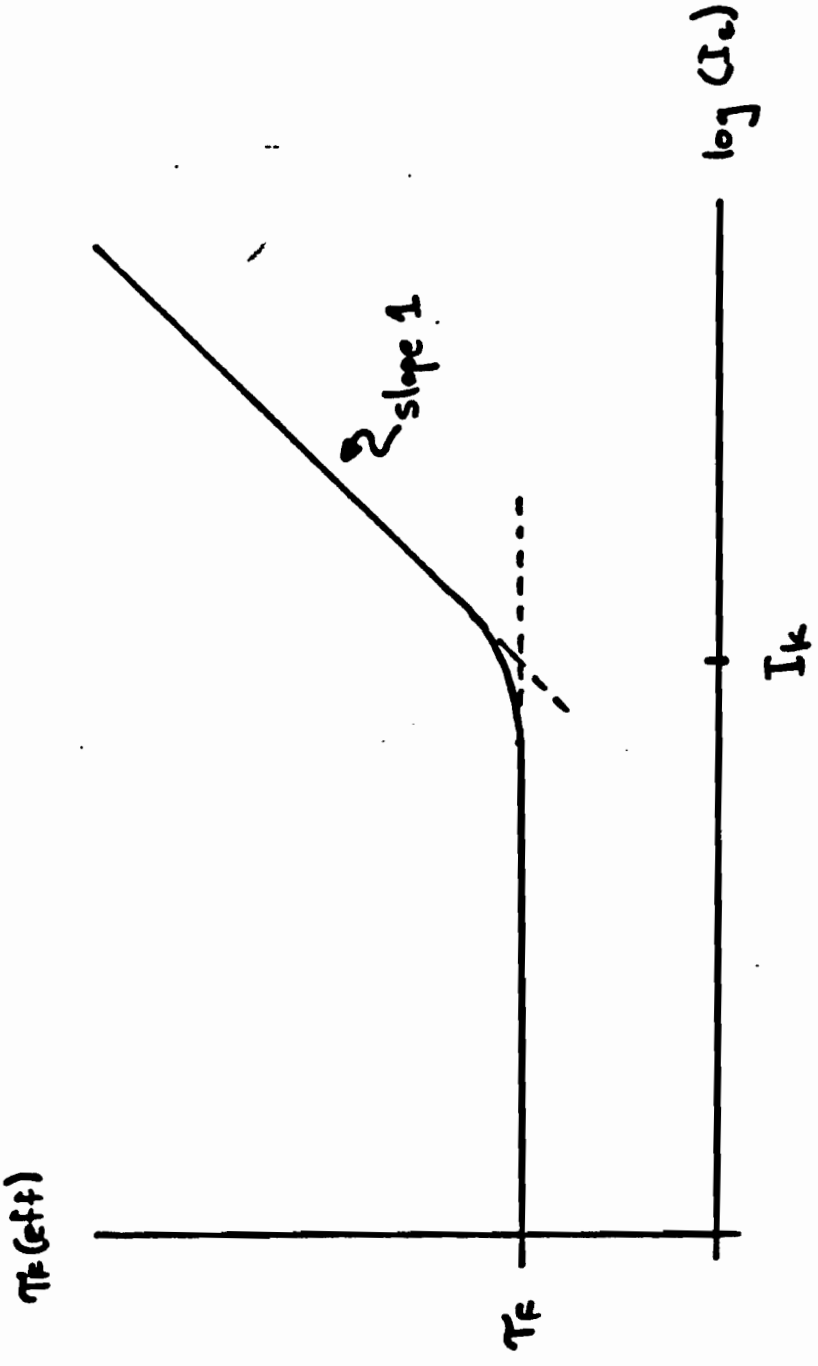


Figure 7

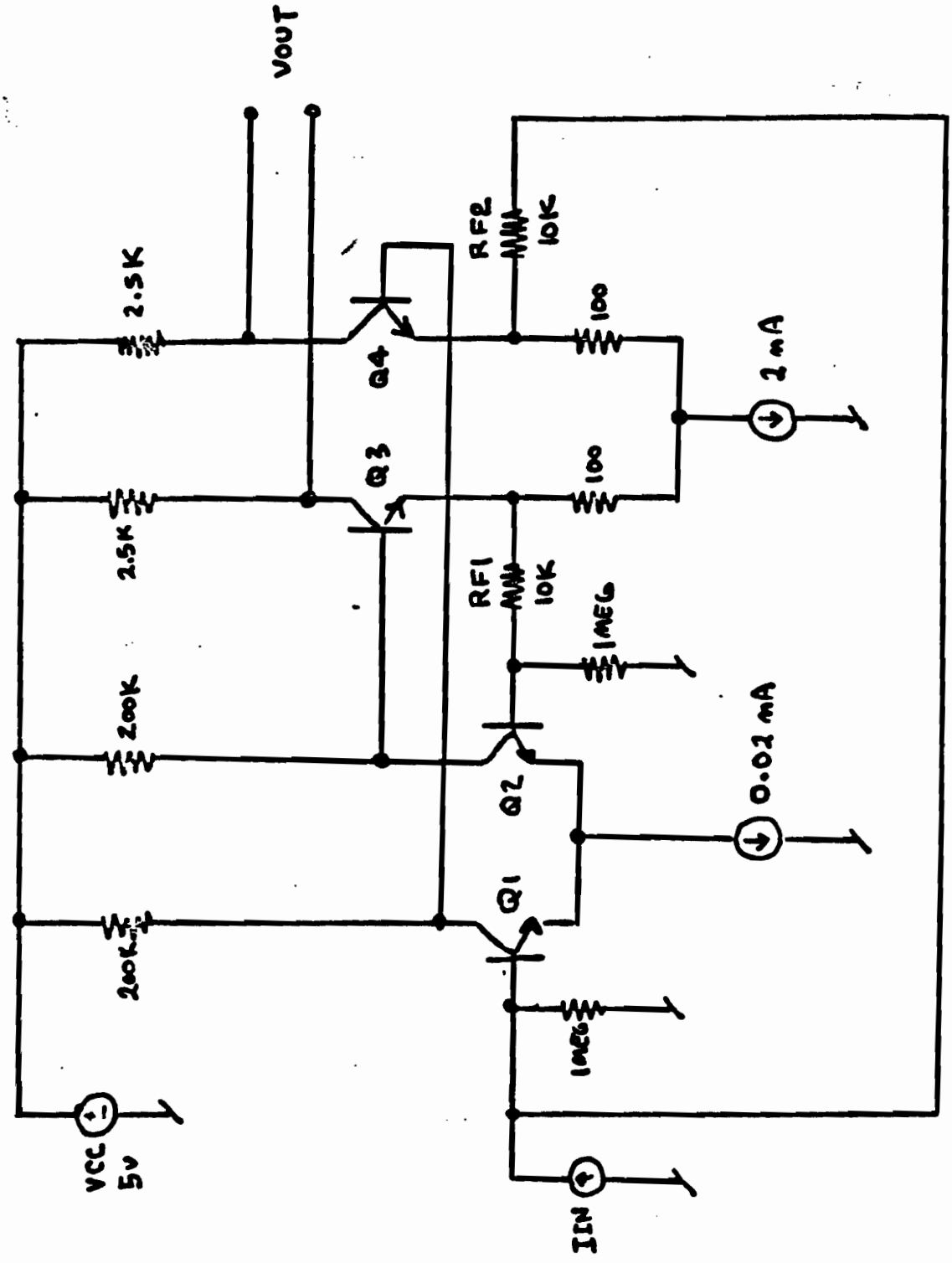

VOUT
RF2
10K
2.5K
100
Q4
2 mA
Q3
100
2.5K
RF1
10K
1MEG
200K
0.02 mA
Q2
Q1
200K
1MEG
VCC
5v
IIN

Figure 8

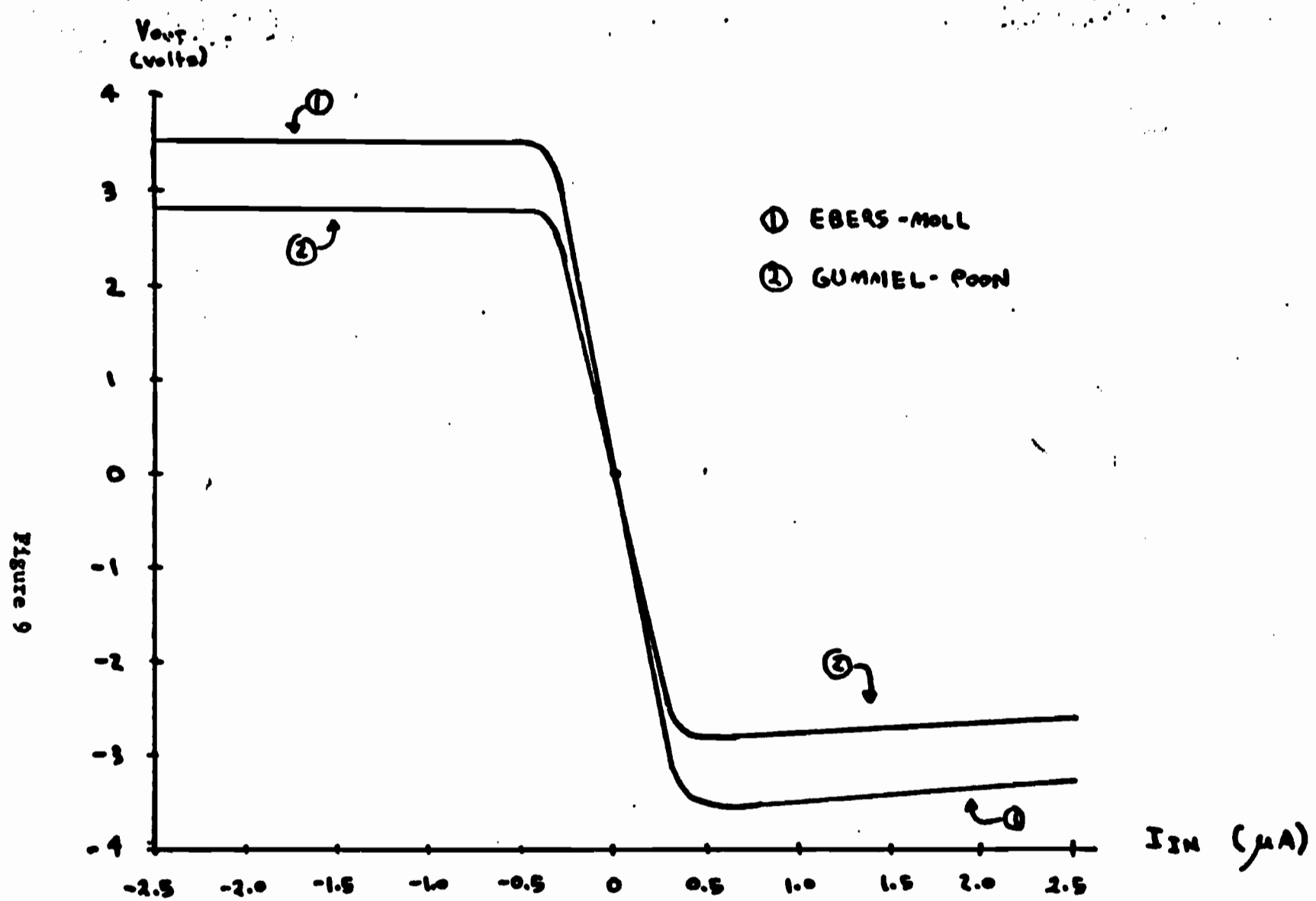

Vout (volts)
4
3
2
1
0
-1
-2
-3
-4
-2.5
-2.0
-1.5
-1.0
-0.5
0
0.5
1.0
1.5
2.0
2.5
IIN (μA)
① EBERS-MOLL
② GUMMEL-POON
①
②
③

Figure 9

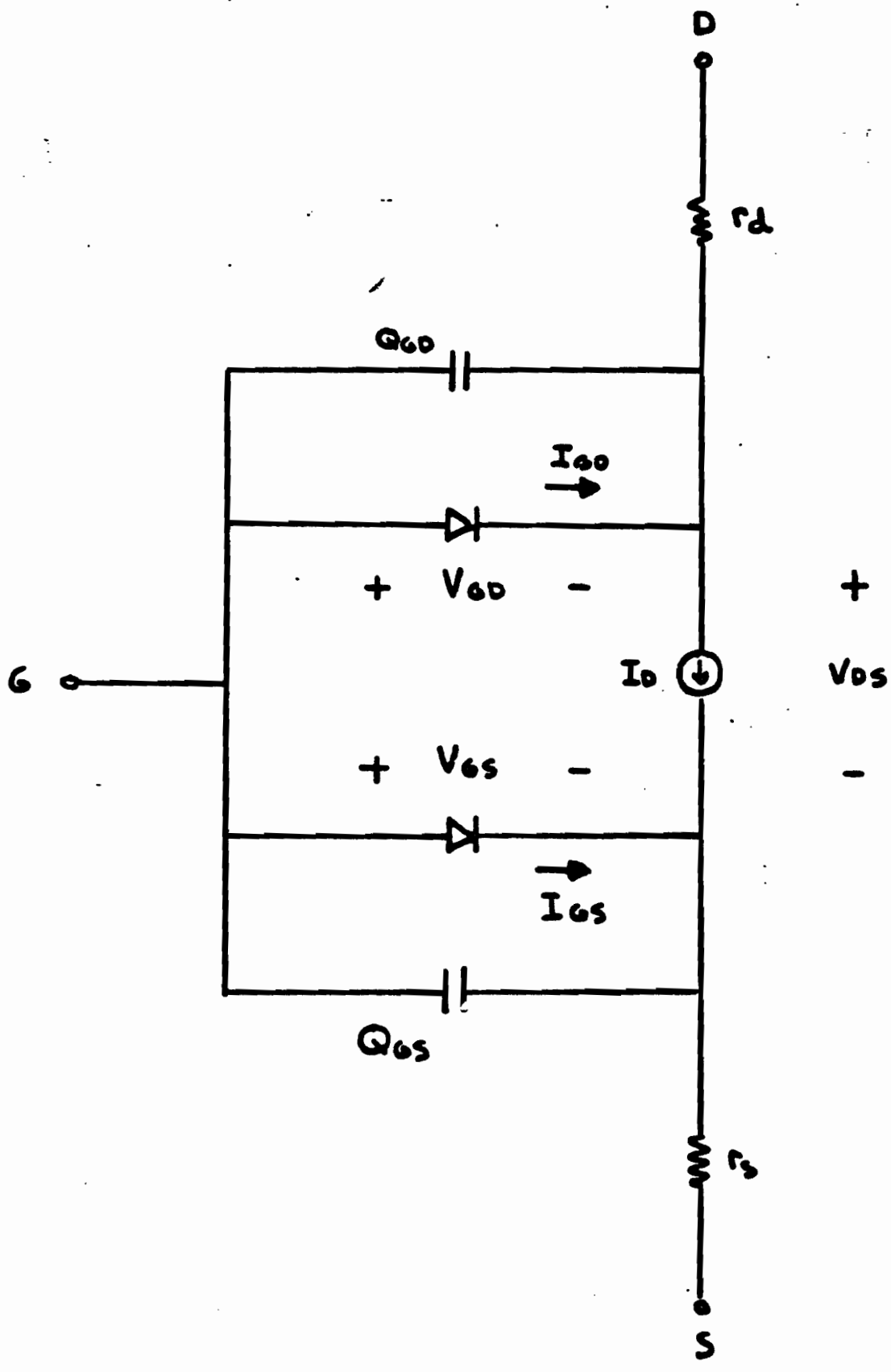


Figure 10

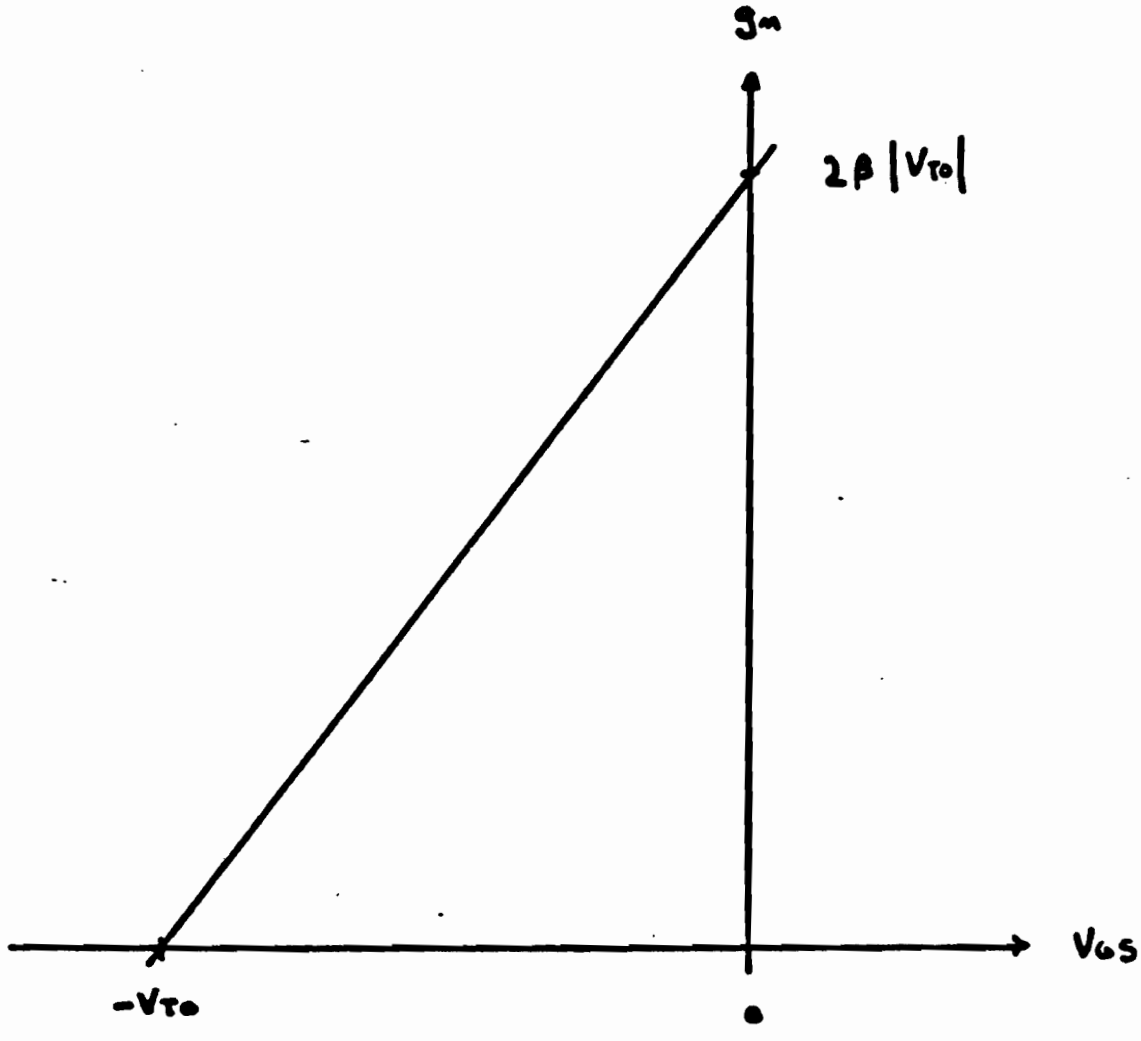


Figure 11

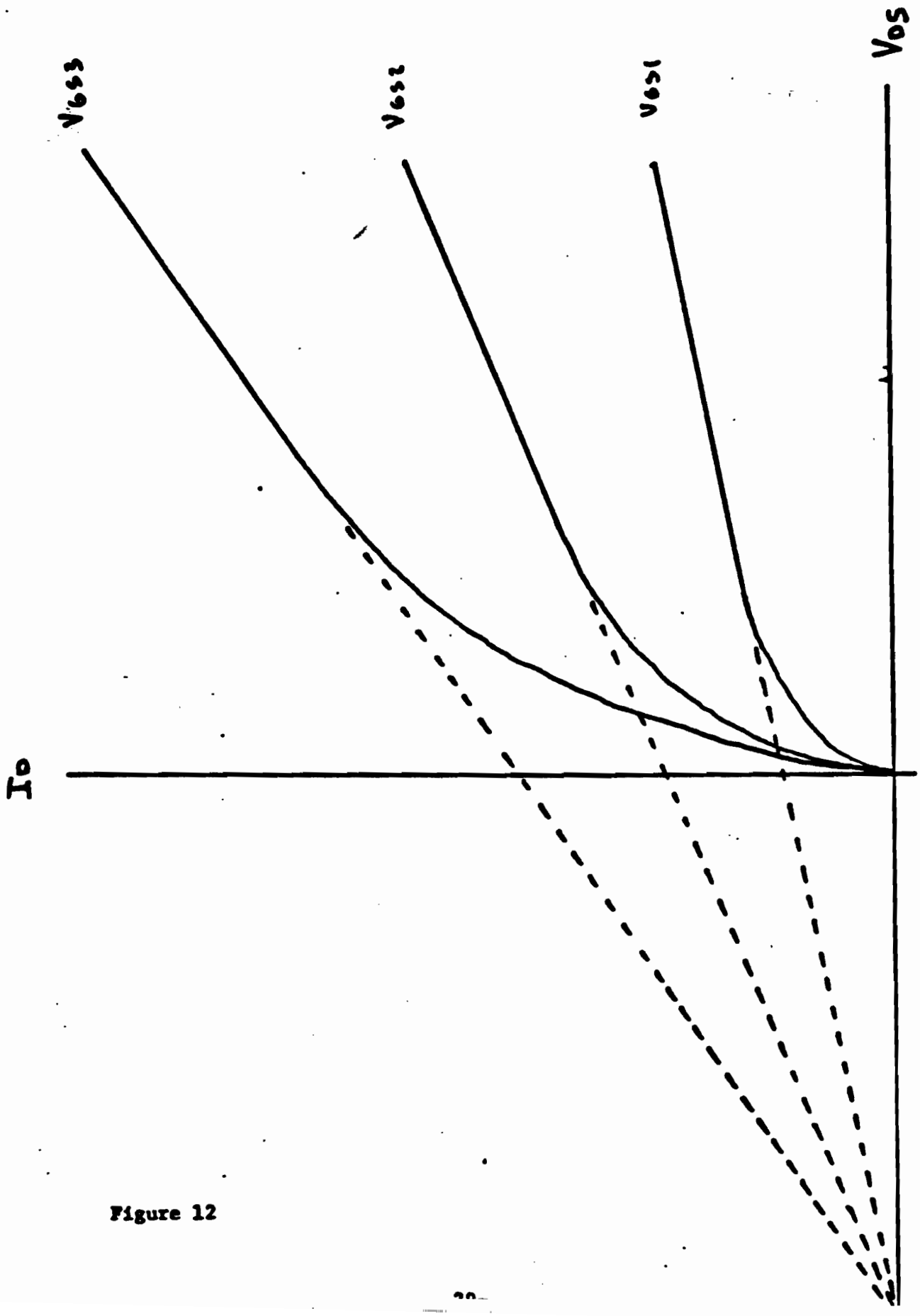


Figure 12

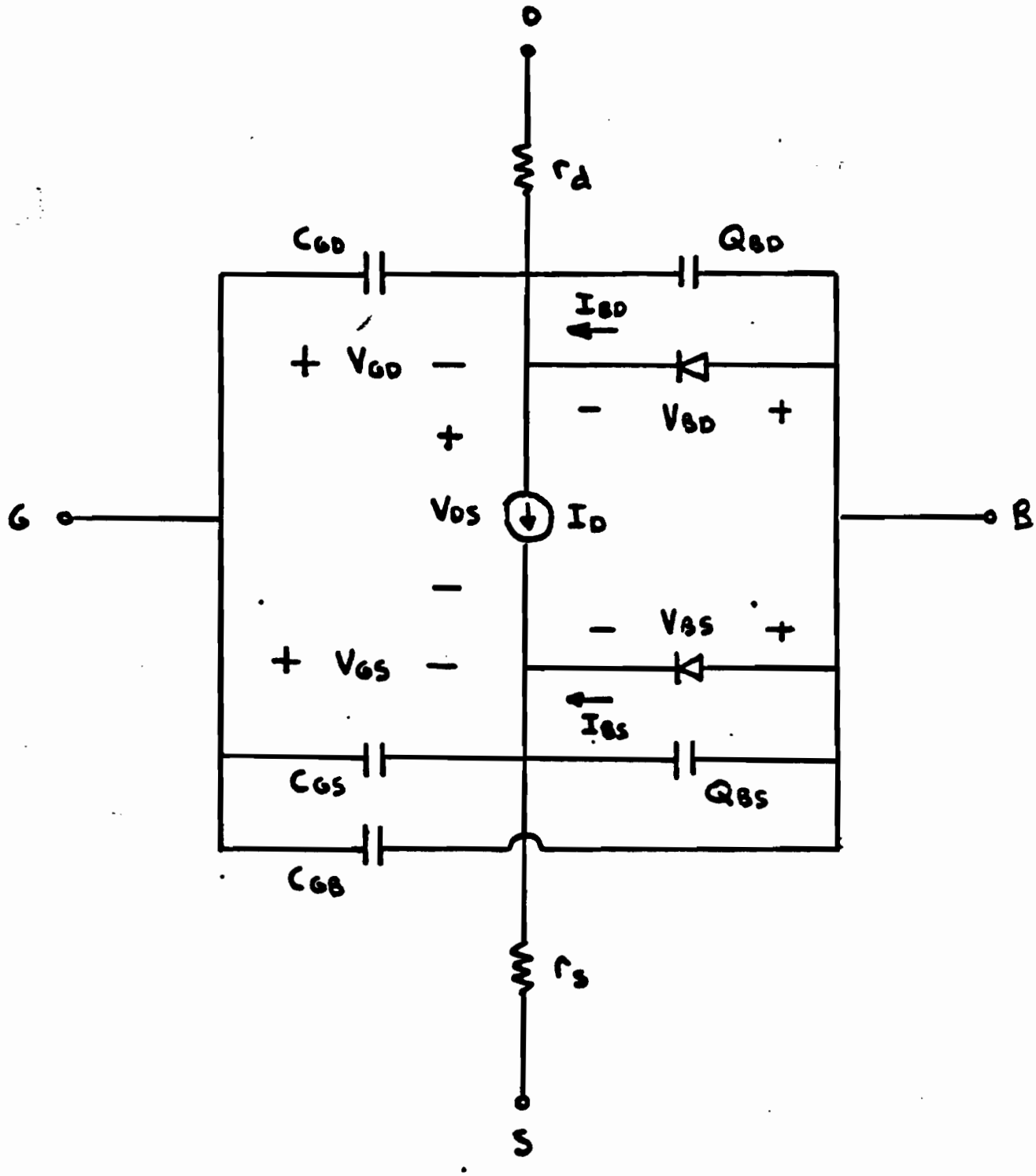
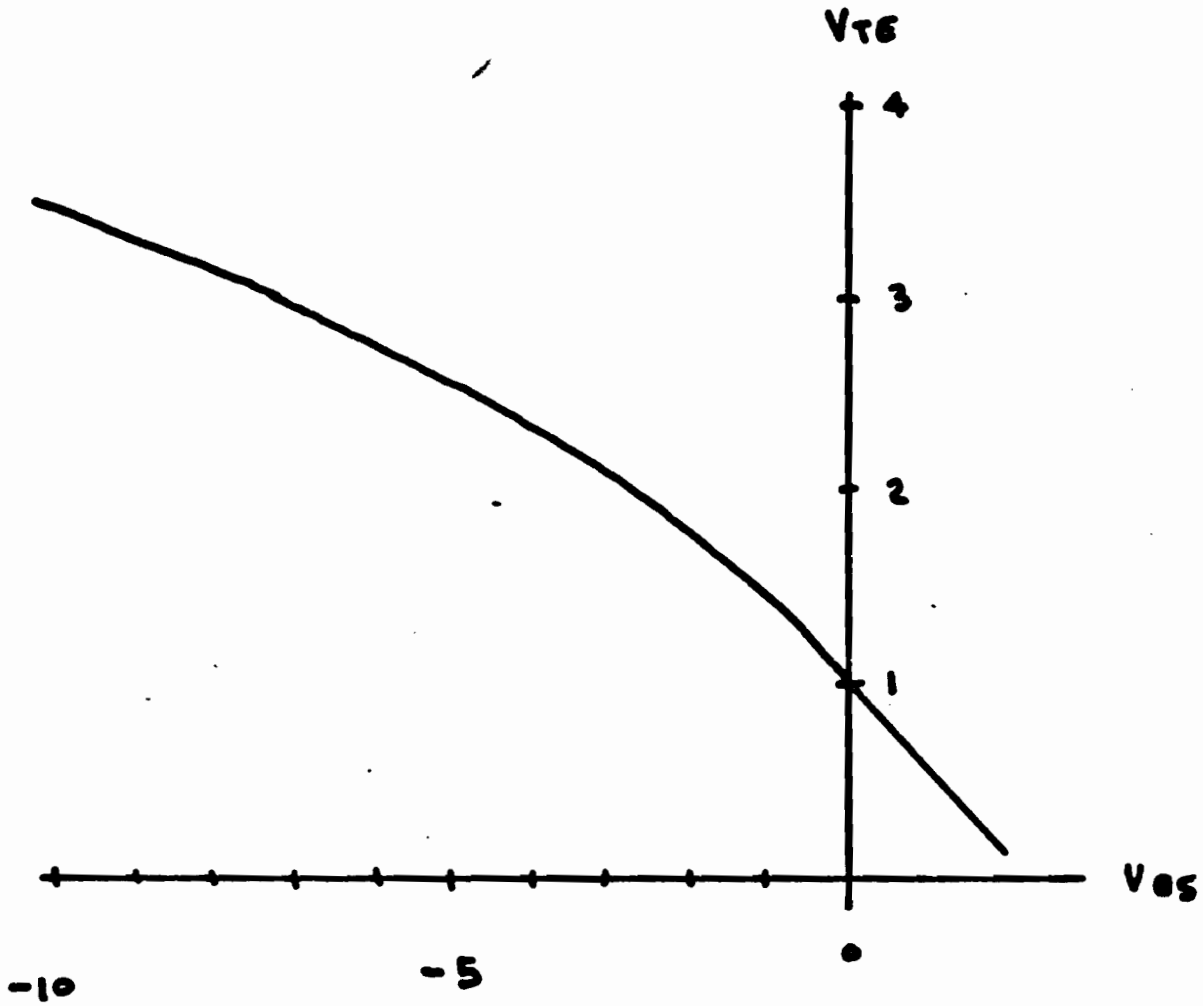


Figure 13



$V_{TO} = 1$ volt

$\gamma = 1 \frac{1}{\sqrt{\text{volt}}}$

$\phi = 0.7$ volt

Figure 14

APPENDIX

UNIVERSITY OF CALIFORNIA
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING
AND COMPUTER SCIENCES

L W NAGEL
D O PEDERSON

25 APR 73

USERS GUIDE FOR SPICE 1

SPICE IS A GENERAL PURPOSE CIRCUIT SIMULATION PROGRAM FOR NONLINEAR DC, NONLINEAR TRANSIENT, AND LINEAR AC ANALYSIS. CIRCUITS MAY CONTAIN RESISTORS, CAPACITORS, INDUCTORS, INDEPENDENT VOLTAGE AND CURRENT SOURCES, VOLTAGE DEPENDENT CURRENT SOURCES, AND THE FOUR MOST COMMON SEMICONDUCTOR DEVICES: BJTS, DIODES, JFETS AND MOSFETS.

SPICE HAS BUILT-IN MODELS FOR THE SEMICONDUCTOR DEVICES, AND THE USER SPECIFIES ONLY THE PERTINENT MODEL PARAMETER VALUES. TWO MODELS ARE AVAILABLE FOR THE BJT. THE SIMPLER MODEL IS BASED ON THE EBERS-MOLL MODEL AND INCLUDES CHARGE STORAGE EFFECTS, OHMIC RESISTANCES, AND A CURRENT DEPENDENT OUTPUT CONDUCTANCE. A MODEL BASED ON THE INTEGRAL CHARGE MODEL OF GUMMEL AND POON IS ALSO AVAILABLE FOR PROBLEMS WHICH REQUIRE A MORE SOPHISTICATED BJT MODEL. THE DIODE MODEL CAN BE USED FOR EITHER JUNCTION DIODES OR SHOTTKY BARRIER DIODES. THE JFET AND MOSFET MODELS ARE BOTH BASED ON THE FET MODEL OF SHICHMAN AND HODGES.

PROGRAM LIMITATIONS

400	NODES, INCLUDING INTERNAL DEVICE NODES. EACH NONZERO OHMIC RESISTANCE IN A DEVICE WILL GENERATE AN INTERNAL NODE. FOR EXAMPLE, A CIRCUIT WITH 35 USER SPECIFIED NODES AND 10 BJTS WITH NONZERO BASE AND COLLECTOR RESISTANCES WILL CONTAIN 55 NODES.
100	DEVICES (BJTS, DIODES, JFETS, AND MOSFETS).
25	INDEPENDENT VOLTAGE OR CURRENT SOURCES. ONLY 5 INDEPENDENT SOURCES CAN BE TIME DEPENDENT FOR TRANSIENT ANALYSIS.
200	TOTAL ELEMENTS, INCLUDING DEVICES AND INDEPENDENT SOURCES.
10	OUTPUT VARIABLES. AN OUTPUT VARIABLE IS EITHER A NODE TO NODE VOLTAGE OR A CURRENT THROUGH AN INDEPENDENT VOLTAGE SOURCE. OUTPUT VARIABLES MAY BE PRINTED IN TABULAR FORM, PLOTTED AS LINE PRINTER PLOTS, OR BOTH. ONLY 5 OUTPUT VARIABLES CAN BE USED IN THE AC SMALL SIGNAL ANALYSIS.
20	SETS OF MODEL PARAMETERS FOR DEVICES.

TYPES OF ANALYSIS

----- DC ANALYSIS

THE DC ANALYSIS PORTION OF SPICE DETERMINES THE DC OPERATING POINT OF THE CIRCUIT WITH INDUCTORS SHORTED AND CAPACITORS OPENED. A DC ANALYSIS IS AUTOMATICALLY PERFORMED PRIOR TO A TRANSIENT ANALYSIS TO DETERMINE THE TRANSIENT INITIAL CONDITIONS, AND PRIOR TO AN AC SMALL SIGNAL ANALYSIS TO DETERMINE THE LINEARIZED, SMALL SIGNAL MODELS FOR NONLINEAR DEVICES. IF REQUESTED, THE DC SMALL SIGNAL VALUE OF A TRANSFER FUNCTION (RATIO OF OUTPUT VARIABLE TO INPUT SOURCE), INPUT RESISTANCE, AND OUTPUT RESISTANCE WILL ALSO BE COMPUTED AS A PART OF THE SMALL SIGNAL OPERATING POINT. THE DC ANALYSIS CAN ALSO BE USED TO GENERATE DC TRANSFER CURVES. A SPECIFIED INDEPENDENT VOLTAGE OR CURRENT SOURCE IS STEPPED OVER A USED SPECIFIED RANGE AND THE DC OUTPUT VARIABLES ARE STORED FOR EACH SEQUENTIAL SOURCE VALUE. THE DC ANALYSIS OPTIONS ARE SPECIFIED ON THE .DC CONTROL CARD (PAGE 15).

----- AC SMALL SIGNAL ANALYSIS

THE AC SMALL SIGNAL PORTION OF SPICE COMPUTES THE AC OUTPUT VARIABLES AS A FUNCTION OF FREQUENCY. THE PROGRAM FIRST COMPUTES THE DC OPERATING POINT OF THE CIRCUIT AND DETERMINES LINEARIZED, SMALL SIGNAL MODELS FOR ALL OF THE NONLINEAR DEVICES IN THE CIRCUIT. THE RESULTANT LINEAR CIRCUIT IS THEN ANALYZED OVER A USER SPECIFIED RANGE OF FREQUENCIES. THE DESIRED OUTPUT OF AN AC SMALL SIGNAL ANALYSIS IS USUALLY A TRANSFER FUNCTION (VOLTAGE GAIN, TRANSIMPEDANCE, ETC). IF THE CIRCUIT HAS ONLY ONE AC INPUT, IT IS CONVENIENT TO SET THAT INPUT TO UNITY AND ZERO PHASE, SO THAT OUTPUT VARIABLES HAVE THE SAME VALUE AS THE TRANSFER FUNCTION OF THE OUTPUT VARIABLE WITH RESPECT TO THE INPUT.

THE GENERATION OF WHITE NOISE BY RESISTORS AND SEMICONDUCTOR DEVICES CAN ALSO BE SIMULATED WITH THE AC SMALL SIGNAL PORTION OF SPICE. EQUIVALENT NOISE SOURCE VALUES ARE DETERMINED AUTOMATICALLY FROM THE SMALL SIGNAL OPERATING POINT OF THE CIRCUIT, AND THE CONTRIBUTION OF EACH NOISE SOURCE IS ADDED AT A GIVEN SUMMING POINT. THE TOTAL OUTPUT NOISE LEVEL AND THE EQUIVALENT INPUT NOISE LEVEL ARE DETERMINED AT EACH FREQUENCY POINT. THE OUTPUT AND INPUT NOISE LEVELS ARE NORMALIZED WITH RESPECT TO THE SQUARE ROOT OF THE NOISE BANDWIDTH AND HAVE THE UNITS VOLTS/RT HZ OR AMPS/RT HZ. THE OUTPUT NOISE AND EQUIVALENT INPUT NOISE CAN BE PRINTED OR PLOTTED IN THE SAME FASHION AS OTHER OUTPUT VARIABLES.

THE FREQUENCY RANGE AND THE NOISE ANALYSIS OPTIONS ARE SPECIFIED ON THE .AC CONTROL CARD (PAGE 15).

----- TRANSIENT ANALYSIS

THE TRANSIENT ANALYSIS PORTION OF SPICE COMPUTES THE TRANSIENT OUTPUT VARIABLES AS A FUNCTION OF TIME OVER A USER SPECIFIED TIME INTERVAL. THE INITIAL CONDITIONS ARE AUTOMATICALLY DETERMINED BY A DC ANALYSIS. ALL SOURCES WHICH ARE NOT TIME DEPENDENT (FOR EXAMPLE, POWER SUPPLIES) ARE SET TO THEIR DC VALUE. FOR LARGE SIGNAL SINUSOIDAL SIMULATIONS, A FOURIER ANALYSIS OF THE OUTPUT WAVEFORM CAN BE SPECIFIED TO OBTAIN THE FREQUENCY DOMAIN FOURIER COEFFICIENTS. THE TRANSIENT TIME INTERVAL AND THE FOURIER ANALYSIS OPTIONS ARE SPECIFIED ON THE .TRAN CONTROL CARD (PAGE 16).

ANALYSIS AT DIFFERENT TEMPERATURES

ALL INPUT DATA FOR SPICE IS ASSUMED TO HAVE BEEN MEASURED AT 27 DEG C (300 DEG K). THE SIMULATION ALSO ASSUMES A NOMINAL TEMPERATURE OF 27 DEG C. THE CIRCUIT CAN BE SIMULATED AT UP TO 5 DIFFERENT TEMPERATURES BY USING A .TEMP CONTROL CARD (PAGE 15).

TEMPERATURE APPEARS EXPLICITLY IN THE EXPONENTIAL TERMS OF THE BJT AND DIODE MODEL EQUATIONS. IN ADDITION, SATURATION CURRENTS HAVE A BUILT-IN TEMPERATURE DEPENDENCE. THE TEMPERATURE DEPENDENCE OF THE SATURATION CURRENT IN THE BJT MODELS IS DETERMINED BY:

```
IS (TEMP) = IO * (TEMP**3) * EXP (-Q * EG / (K * TEMP)),
```

WHERE K IS BOLTZMANS CONSTANT, Q IS THE ELECTRONIC CHARGE, IO IS A CONSTANT, AND EG IS THE ENERGY GAP WHICH IS A MODEL PARAMETER. THE TEMPERATURE DEPENDENCE OF THE SATURATION CURRENT IN THE JUNCTION DIODE MODEL IS DETERMINED BY:

```
IS (TEMP) = IO * (TEMP**(3/N)) * EXP (-Q * EG / (K * TEMP)),
```

WHERE N IS THE EMISSION COEFFICIENT, WHICH IS A MODEL PARAMETER, AND THE OTHER SYMBOLS HAVE THE SAME MEANING AS ABOVE. FOR SHOTTKY BARRIER DIODES, THE TEMPERATURE DEPENDENCE OF THE SATURATION CURRENT IS DETERMINED BY:

```
IS (TEMP) = IO * (TEMP**(2/N)) * EXP (-Q * EG / (K * TEMP)).
```

CONVERGENCE

BOTH DC AND TRANSIENT SOLUTIONS ARE OBTAINED BY AN ITERATIVE PROCESS WHICH IS TERMINATED WHEN THE NODE VOLTAGES CONVERGE TO WITHIN A TOLERANCE OF 0.1 PERCENT OR 50 MICROVOLTS, WHICHEVER IS LARGER. ALTHOUGH THE PARTICULAR ALGORITHM USED IS SPICE HAS BEEN FOUND TO BE VERY RELIABLE, IN SOME CASES IT WILL FAIL TO CONVERGE TO A SOLUTION. WHEN THIS HAPPENS, THE PROGRAM WILL PRINT OUT THE LAST NODE VOLTAGES AND TERMINATE THE JOB. THE NODE VOLTAGES THAT ARE PRINTED ARE NOT NECESSARILY CORRECT OR EVEN CLOSE TO THE CORRECT SOLUTION.

FAILURE TO CONVERGE IN THE DC ANALYSIS IS USUALLY DUE TO AN ERROR IN SPECIFYING CIRCUIT CONNECTIONS, ELEMENT VALUES, OR MODEL PARAMETER VALUES. REGENERATIVE SWITCHING CIRCUITS OR CIRCUITS WITH POSITIVE FEEDBACK PROBABLY WILL NOT CONVERGE IN THE DC ANALYSIS. FAILURE TO CONVERGE IN THE TRANSIENT ANALYSIS CAN ALSO BE DUE TO A TIME STEP WHICH IS TOO LARGE. SPICE PRESENTLY DOES NOT HAVE AN AUTOMATIC TIME STEP CONTROL, AND SIGNIFICANT ERROR AND/OR NONCONVERGENCE CAN RESULT IF THE TIME STEP IS LARGE COMPARED TO THE CIRCUIT TIME CONSTANTS.

INPUT FORMAT

THE INPUT FORMAT FOR SPICE IS OF THE FREE FORMAT TYPE. FIELDS ON A CARD ARE SEPARATED BY ONE OR MORE BLANKS, A COMMA, OR AN EQUAL (=) SIGN. SPACES PRECEDING OR FOLLOWING A COMMA OR EQUAL SIGN ARE IGNORED. A CARD MAY BE CONTINUED ONTO THE FOLLOWING CARD BY PUNCHING A + BEFORE THE FIRST FIELD ON THE CONTINUATION CARD.

A NAME FIELD MUST BEGIN WITH A LETTER (A THRU Z) AND CANNOT CONTAIN COMMAS OR BLANKS. ONLY THE FIRST SEVEN CHARACTERS OF THE NAME ARE USED.

A NUMBER FIELD MAY BE AN INTEGER FIELD (12,-44), A FLOATING POINT FIELD (3.141593), EITHER AN INTEGER OR A FLOATING POINT NUMBER FOLLOWED BY AN INTEGER EXPONENT (1E-14, 2.65E3), OR EITHER AN INTEGER OR A FLOATING POINT NUMBER FOLLOWED BY ONE OF THE FOLLOWING SCALE FACTORS:

G	1.0E9
MEG	1.0E6
K	1.0E3
M	1.0E-3
U	1.0E-6
N	1.0E-9
P	1.0E-12

LETTERS IMMEDIATELY FOLLOWING A NUMBER THAT ARE NOT SCALE FACTORS ARE IGNORED, AND LETTERS IMMEDIATELY FOLLOWING A SCALE FACTOR ARE IGNORED. HENCE, 10, 10V, 10VOLTS, AND 10HZ ALL REPRESENT THE SAME NUMBER, AND M, MA, MSEC, AND MMHOS ALL REPRESENT THE SAME SCALE FACTOR. NOTE THAT 1000, 1000.0, 1000HZ, 1E3, 1.0E3, 1KHZ, AND 1K ALL REPRESENT THE SAME NUMBER.

CIRCUIT DESCRIPTION

THE CIRCUIT TO BE ANALYZED IS DESCRIBED TO SPICE BY A SET OF ELEMENT CARDS, WHICH DEFINE THE CIRCUIT TOPOLOGY AND ELEMENT VALUES, AND A SET OF CONTROL CARDS, WHICH DEFINE THE MODEL PARAMETERS AND THE RUN CONTROLS. THE FIRST CARD IN THE INPUT DECK MUST BE A TITLE CARD, AND THE LAST CARD MUST BE A .END CARD. THE ORDER OF THE REMAINING CARDS IS ARBITRARY.

NODE NUMBERS MUST BE INTEGERS. THE DATUM NODE MUST BE NUMBERED 0 (ZERO). NODES NEED NOT BE NUMBERED SEQUENTIALLY. THE CIRCUIT CANNOT CONTAIN A LOOP OF VOLTAGE SOURCES AND/OR INDUCTORS AND CANNOT CONTAIN A CUTSET OF CURRENT SOURCES AND/OR CAPACITORS. EACH NODE IN THE CIRCUIT, INCLUDING THE DATUM NODE, MUST HAVE AT LEAST TWO CONNECTIONS.

ELEMENT CARDS

***** RESISTORS, CAPACITORS, INDUCTORS

GENERAL FORM
```
RXXXXXX N1 N2 VALUE
CXXXXXX N1 N2 VALUE
LXXXXXX N1 N2 VALUE
```

EXAMPLES
```
R13 12 17 1K
CGOOD 13 0 10P
LLINKS 42 69 1U
```

N1 AND N2 ARE THE TWO ELEMENT NODES. THE ORDER OF THE NODES FOR THESE ELEMENTS IS UNIMPORTANT. VALUE IS THE RESISTANCE (OHMS), THE CAPACITANCE (FARADS), AND THE INDUCTANCE (HENRIES), RESPECTIVELY. THIS VALUE CANNOT BE NEGATIVE OR ZERO.

***** VOLTAGE CONTROLLED CURRENT SOURCES

GENERAL FORM
```
GXXXXXX V N+ N- NC+ NC- VALUE DELAY
```

EXAMPLES
```
GSORS V 13 12 14 12 1.0M
GM V 1 20 4 20 -2.0M 3.0NS
```

THE LETTER V MUST BE IN THE FIELD FOLLOWING THE ELEMENT NAME. N+ AND N- ARE THE POSITIVE AND NEGATIVE NODES, RESPECTIVELY. CURRENT FLOWS FROM THE POSITIVE NODE, THRU THE SOURCE, TO THE NEGATIVE NODE. NC+ AND NC- ARE THE POSITIVE AND NEGATIVE CONTROLLING NODES, RESPECTIVELY. VALUE IS THE TRANSCONDUCTANCE (MHOS).

IN THE AC ANALYSIS THE TRANSCONDUCTANCE CAN BE MODIFIED BY AN OPTIONAL DELAY (LINEAR PHASE) OPERATOR. THE DELAY (SECONDS) IS APPENDED AFTER THE VALUE. IF A DELAY, TD, IS INCLUDED, THE COMPLEX, FREQUENCY DEPENDENT VALUE OF TRANSCONDUCTANCE IS DETERMINED BY:

$$GM = VALUE * EXP(-J * 6.28318 * FREQ * TD)$$

THE DELAY IS IGNORED IN THE DC AND TRANSIENT ANALYSES.

***** INDEPENDENT SOURCES

GENERAL FORM VXXXXXX N+ N- DC DCVAL AC ACVAL PHASE
              IXXXXXX N+ N- DC DCVAL AC ACVAL PHASE

EXAMPLES VCC 10 0 DC 6
          IZENER 13 15 DC 600MA
          VIN 13 2 DC 0.001 AC 1
          IIN 21 23 AC 0.333 45.0
          VMEAS 12 9

N+ IS THE POSITIVE NODE AND N- IS THE NEGATIVE NODE. NOTE THAT VOLTAGE SOURCES NEED NOT BE GROUNDED. CURRENT FLOWS FROM THE POSITIVE NODE, THRU THE SOURCE, TO THE NEGATIVE NODE.

DCVAL IS THE DC VALUE OF THE SOURCE. THE SOURCE IS SET TO THIS VALUE FOR DC ANALYSIS AND, IF NO TIME DEPENDENCE IS ATTACHED, IN THE TRANSIENT ANALYSIS. IF THE DC SOURCE VALUE IS ZERO, THE LETTERS DC AND THE DC VALUE CAN BE OMITTED.

ACVAL IS THE AC VALUE AND PHASE IS THE AC PHASE. THE SOURCE IS SET TO THIS VALUE IS THE AC ANALYSIS. THE ARBITRARY PHASE FACTOR CAN BE OMITTED. IF THE SOURCE IS NOT AN AC SMALL SIGNAL INPUT, THE LETTERS AC AND THE AC VALUES ARE OMITTED.

A SOURCE MAY BE GIVEN A TIME DEPENDENCE FOR THE TRANSIENT ANALYSIS BY APPENDING ONE OF THE THREE PREDEFINED FUNCTIONS: PULSE, EXPONENTIAL, AND SINUSOIDAL. IF PARAMETERS OTHER THAN SOURCE VALUES ARE OMITTED OR SET TO ZERO, THE DEFAULT VALUES SHOWN WILL BE ASSUMED. TSTEP IS THE PRINTING INCREMENT (TIME STEP), AND TSTOP IS THE FINAL TIME (PAGE 15).

1. PULSE PULSE V1 V2 TD TR TF PW PER

EXAMPLE VIN 3 0 PULSE -1 1 2NS 2NS 2NS 50NS 100NS

PARAMETERS AND DEFAULT VALUES

V1	INITIAL VALUE	---
V2	PULSED VALUE	---
TD	DELAY TIME	TSTEP
TR	RISE TIME	TSTEP
TF	FALL TIME	TSTEP
PW	WIDTH	TSTOP
PER	PERIOD	TSTOP

A SINGLE PULSE IS DESCRIBED BY THE FOLLOWING PIECEWISE LINEAR TABLE.

TIME	VALUE
0	V1
TD	V1
TD+TR	V2
TD+TR+PW	V2
TD+TR+PW+TF	V1
TSTOP	V1

2. EXPONENTIAL EXP V1 V2 TD1 TAU1 TD2 TAU2

EXAMPLE VIN 3 0 EXP -4 -1 2NS 30NS 60NS 40NS

PARAMETERS AND DEFAULT VALUES

V1	INITIAL VALUE	---
V2	PULSED VALUE	---
TD1	RISE DELAY TIME	TSTEP
TAU1	RISE TIME CONSTANT	TSTEP
TD2	FALL DELAY TIME	TSTEP
TAU2	FALL TIME CONSTANT	TSTEP

TIME	VALUE
0 TO TD1	V1
TD1 TO TD2	V1+(V2-V1)(1-EXP(-(T-TD1)/TAU1))
TD2 TO TSTOP	V1+(V2-V1)(1-EXP(-(T-TD1)/TAU1))+(V1-V2)(1-EXP(-(T-TD2)/TAU2))

3. SINUSOIDAL SIN VO VA FREQ TD THETA

EXAMPLE VIN 3 0 SIN 0 1 100MEG 1NS 1E10

PARAMETERS AND DEFAULT VALUES

VO	OFFSET	---
VA	AMPLITUDE	---
FREQ	FREQUENCY (IN HZ)	1/TSTOP
TD	DELAY	TSTEP
THETA	DAMPING FACTOR	0

TIME	VALUE
0 TO TD	VO
TD TO TSTOP	VO + VA * EXP(-(T-TD) * THETA) * SINE (6.28318 * FREQ * T)

SOURCES MAY BE GIVEN ANY COMBINATION OF VALUES (DC, AC, OR TRANSIENT), AND THESE VALUES MAY BE SPECIFIED IN ANY ORDER AS LONG AS THEY FOLLOW THE PROPER KEY WORD.

EXAMPLES VIN 13 12 SIN 0 1 10MEG DC 0.1 AC 1 45
IZ 19 0 DC 0 PULSE 0 1 AC 0.5
VEO 12 0 DC 0.5 EXP 0.5 0.9 10NS 40NS 70NS 40NS AC 1

***** BIPOLAR JUNCTION TRANSISTORS

GENERAL FORM QXXXXXX NC NB NE MNAME AREA

EXAMPLE QAMP33 7 9 1 MOD1 2.0

NC IS THE COLLECTOR NODE, NB IS THE BASE NODE, NE IS THE EMITTER NODE, MNAME IS THE MODEL NAME (PAGE 9) AND AREA IS THE AREA FACTOR. THE AREA FACTOR IS EQUIVALENT TO THE NUMBER OF PARALLEL DEVICES. AN AREA FACTOR OF 2.0 IMPLIES THAT TWO TRANSISTORS OF THE SAME MODEL ARE CONNECTED IN PARALLEL. IF THE AREA IS OMITTED, AN AREA FACTOR OF 1.0 IS ASSUMED.

***** JUNCTION DIODES

GENERAL FORM DXXXXXX N+ N- MNAME AREA

EXAMPLE DBRIDGE 8 10 DIODE1

N+ IS THE POSITIVE NODE, N- IS THE NEGATIVE NODE, MNAME IS THE MODEL NAME (PAGE 9), AND AREA IS THE AREA FACTOR (SEE BJTS, ABOVE).

***** JUNCTION FIELD EFFECT TRANSISTORS

GENERAL FORM JXXXXXX ND NG NS MNAME AREA

EXAMPLE J1 7 2 3 JN1

ND IS THE DRAIN NODE, NG IS THE GATE NODE, NS IS THE SOURCE NODE, MNAME IS THE MODEL NAME(PAGE 9), AND AREA IS THE AREA FACTOR (SEE BJTS, ABOVE).

***** MOSFETS

GENERAL FORM MXXXXXX ND NG NS NB MNAME AREA

EXAMPLE M31G 2 3 4 7 MLONG

ND IS THE DRAIN NODE, NG IS THE GATE NODE, NS IS THE SOURCE NODE, NB IS THE BULK (SUBSTRATE) NODE, MNAME IS THE MODEL NAME (PAGE 9), AND AREA IS THE AREA FACTOR (SEE BJTS, ABOVE).

***** .MODEL CARD

GENERAL FORM .MODEL MNAME TYPE PNAME1=PVAL1 PNAME2=PVAL2 ...

EXAMPLE .MODEL MOD1 NPN BF=50 IS=1E-13 VA=50

THE .MODEL CARD SPECIFIES A SET OF MODEL PARAMETERS THAT WILL BE USED BY ONE OR MORE DEVICES. MNAME IS THE MODEL NAME, AND TYPE IS ONE OF THE FOLLOWING TEN TYPES:

NPN	NPN EBERS-MOLL BJT MODEL
PNP	PNP EBERS-MOLL BJT MODEL
NGP	NPN GUMMEL-POON BJT MODEL
PGP	PNP GUMMEL-POON BJT MODEL
D	JUNCTION DIODE MODEL
SBD	SHOTTKY BARRIER DIODE MODEL
NJF	N CHANNEL JFET MODEL
PJF	P CHANNEL JFET MODEL
NMO	N CHANNEL MOSFET MODEL
PMO	P CHANNEL MOSFET MODEL

PARAMETER VALUES ARE DEFINED BY APPENDING THE PARAMETER NAME, AS GIVEN BELOW FOR EACH MODEL TYPE, FOLLOWED BY AN EQUAL SIGN AND THE PARAMETER VALUE. MODEL PARAMETERS THAT ARE NOT GIVEN A VALUE ARE ASSIGNED THE DEFAULT VALUE GIVEN BELOW FOR EACH MODEL TYPE.

MODEL PARAMETER VALUES CAN ALSO BE SPECIFIED AS A STRING OF NUMBERS IN THE ORDER GIVEN BELOW FOR EACH MODEL TYPE. THE FOLLOWING MODEL SPECIFICATION IS EQUIVALENT TO THE PREVIOUS MODEL CARD EXAMPLE:

EXAMPLE .MODEL MOD1 NPN 50,,,,,,,,,,1E-13,,,50

----- DIODE MODELS (BOTH JUNCTION AND SBD)

THE ONLY DIFFERENCE BETWEEN THE JUNCTION DIODE MODEL AND THE SHOTTKY BARRIER DIODE MODEL IS THE TEMPERATURE DEPENDENCE OF SATURATION CURRENT (SEE PAGE 3). THE DC CHARACTERISTICS OF THE DIODE ARE DETERMINED BY THE PARAMETERS IS AND N. AN OHMIC RESISTANCE, RS, IS INCLUDED. CHARGE STORAGE EFFECTS ARE MODELED BY A TRANSIT TIME, TT, AND A NONLINEAR DEPLETION LAYER CAPACITANCE WHICH VARIES AS THE -1/2 POWER OF JUNCTION VOLTAGE AND IS DEFINED BY THE PARAMETERS CJO AND PHI. THE ENERGY GAP, EG, AFFECTS ONLY THE TEMPERATURE DEPENDENCE OF THE SATURATION CURRENT (SEE PAGE 3).

	NAME	PARAMETER	DEFAULT	TYPICAL
1	RS	OHMIC RESISTANCE	0	10
2	TT	TRANSIT TIME	0	0.1NS
3	CJO	ZERO BIAS JUNCTION CAPACITANCE	0	2PF
4	IS	SATURATION CURRENT	1.0E-14	1.0E-14
5	N	EMISSION COEFFICIENT	1	1.0
6	PHI	JUNCTION POTENTIAL	1	0.6
7	EG	ENERGY GAP	1.11 SI 0.69 SBD	1.11 FOR SI 0.69 FOR SBD 0.67 FOR GE

----- EBERS-MOLL BJT MODELS (BOTH NPN AND PNP)

THE EBERS-MOLL BJT MODEL USES THE DC EBERS-MOLL MODEL AS A BASIS. THE DC CHARACTERISTICS OF THE DEVICE ARE DETERMINED BY THE PARAMETERS BF AND BR, THE FORWARD AND REVERSE CURRENT GAINS, VA, WHICH DETERMINES THE OUTPUT CONDUCTANCE, AND THE SATURATION CURRENT, IS. THREE OHMIC RESISTANCES, RB, RC, AND RE, HAVE BEEN INCLUDED. BASE CHARGE STORAGE IS MODELED BY FORWARD AND REVERSE TRANSIT TIMES, TF AND TR, AND NONLINEAR DEPLETION LAYER CAPACITANCES WHICH VARY AS THE -1/2 POWER OF JUNCTION VOLTAGE AND ARE DEFINED BY THE PARAMETERS CJE, PE, CJC, AND PC. A CONSTANT COLLECTOR-SUBSTRATE CAPACITANCE, CCS, IS ALSO INCLUDED. THE ENERGY GAP, EG, AFFECTS ONLY THE TEMPERATURE DEPENDENCE OF THE SATURATION CURRENT (SEE PAGE 3).

	NAME	PARAMETER	DEFAULT	TYPICAL
1	BF	FORWARD BETA	100	100
2	BR	REVERSE BETA	1	0.1
3	RB	BASE OHMIC RESISTANCE	0	100
4	RC	COLLECTOR OHMIC RESISTANCE	0	10
5	RE	EMITTER OHMIC RESISTANCE	0	1
6	CCS	COLLECTOR-SUBSTRATE CAPACITANCE	0	2PF
7	TF	FORWARD TRANSIT TIME	0	0.1NS
8	TR	REVERSE TRANSIT TIME	0	10NS
9	CJE	ZERO BIAS B-E JUNCTION CAPACITANCE	0	2PF
10	CJC	ZERO BIAS B-C JUNCTION CAPACITANCE	0	1PF
11	IS	SATURATION CURRENT	1.0E-14	1.0E-14
12	PE	B-E JUNCTION POTENTIAL	1	0.7
13	PC	B-C JUNCTION POTENTIAL	1	0.5
14	VA	EARLY VOLTAGE	INFINITE	50
15	EG	ENERGY GAP	1.11	1.11 FOR SI 0.67 FOR GE

----- GUMMEL-POON BJT MODELS (BOTH NPN AND PNP)

THE INTEGRAL CHARGE MODEL OF GUMMEL AND POON IS A MORE COMPLICATED AND MORE COMPLETE BJT MODEL FOR PROBLEMS WHICH REQUIRE ACCURATE BJT MODELS. THE DC MODEL IS DEFINED BY THE PARAMETERS BFM, C2, IK, AND NE, WHICH DETERMINE THE FORWARD CURRENT GAIN CHARACTERISTICS, BRM, C4, IKR, AND NC, WHICH DETERMINE THE REVERSE CURRENT GAIN CHARACTERISTICS, VA AND VB, WHICH DETERMINE THE OUTPUT CONDUCTANCE FOR FORWARD AND REVERSE REGIONS, AND THE SATURATION CURRENT, IS. THREE OHMIC RESISTANCES, RB, RC, AND RE, ARE INCLUDED. BASE CHARGE STORAGE IS MODELED BY FORWARD AND REVERSE TRANSIT TIMES, TF AND TR, AND NONLINEAR DEPLETION LAYER CAPACITANCES WHICH ARE DETERMINED BY CJE, PE, AND ME FOR THE B-E JUNCTION, AND CJC, PC, AND MC FOR THE B-C JUNCTION. A CONSTANT COLLECTOR-SUBSTRATE CAPACITANCE, CCS, IS ALSO INCLUDED. THE ENERGY GAP, EG, IS INCLUDED AS IN THE SIMPLER BJT MODEL.

	NAME	PARAMETER	DEFAULT	TYPICAL
1	BFM	SAT CURRENT/IDEAL B-E SAT CURRENT	100	100
2	BRM	SAT CURRENT/IDEAL B-C SAT CURRENT	1	0.1
3	RB	BASE OHMIC RESISTANCE	0	100
4	RC	COLLECTOR OHMIC RESISTANCE	0	10
5	RE	EMITTER OHMIC RESISTANCE	0	1
6	CCS	COLLECTOR-SUBSTRATE CAPACITANCE	0	2PF
7	TF	FORWARD TRANSIT TIME	0	0.1NS
8	TR	REVERSE TRANSIT TIME	0	10NS
9	CJE	ZERO BIAS B-E JUNCTION CAPACITANCE	0	2PF
10	CJC	ZERO BIAS B-C JUNCTION CAPACITANCE	0	1PF
11	IS	SATURATION CURRENT	1.0E-14	1.0E-14
12	VA	FORWARD EARLY VOLTAGE	INFINITE	50
13	VB	REVERSE EARLY VOLTAGE	INFINITE	50
14	C2	NONIDEAL B-E SAT CURRENT/SAT CURRENT	0	1000
15	IK	FORWARD KNEE CURRENT	INFINITE	10MA
16	NE	B-E EMISSION COEFFICIENT	2.0	1.5
17	C4	NONIDEAL B-C SAT CURRENT/SAT CURRENT	0	1.0
18	IKR	REVERSE KNEE CURRENT	INFINITE	100MA
19	NC	B-C EMISSION COEFFICIENT	2.0	1.5
20	PE	B-E JUNCTION POTENTIAL	1.0	0.7
21	ME	B-E GRADING COEFFICIENT	0.5	0.33
22	PC	B-C JUNCTION POTENTIAL	1.0	0.5
23	MC	B-C GRADING COEFFICIENT	0.5	0.33
24	EG	ENERGY GAP	1.11	1.11 FOR SI 0.67 FOR GE

JFET MODELS (BOTH N AND P CHANNEL)

THE JFET MODEL IS DERIVED FROM THE FET MODEL OF SHICHMAN AND HODGES. THE DC CHARACTERISTICS ARE DEFINED BY THE PARAMETERS VTO AND BETA, WHICH DETERMINE THE VARIATION OF DRAIN CURRENT WITH GATE VOLTAGE, LAMBDA, WHICH DETERMINES THE OUTPUT CONDUCTANCE, AND IS, THE SATURATION CURRENT OF THE TWO GATE JUNCTIONS. TWO OHMIC RESISTANCES, RD AND RS, ARE INCLUDED. CHARGE STORAGE IS MODELED BY NONLINEAR DEPLETION LAYER CAPACITANCES FOR BOTH GATE JUNCTIONS WHICH VARY AS THE -1/2 POWER OF JUNCTION VOLTAGE AND ARE DEFINED BY THE PARAMETERS CGS, CGD, AND PB.

	NAME	PARAMETER	DEFAULT	TYPICAL
1	VTO	THRESHOLD VOLTAGE	-2.0	-2.0
2	BETA	TRANSCONDUCTANCE PARAMETER	1.0E-4	1.0E-3
3	LAMBDA	CHANNEL LENGTH MODULATION PARAMETER	0	1.0E-4
4	RD	DRAIN OHMIC RESISTANCE	0	100
5	RS	SOURCE OHMIC RESISTANCE	0	100
6	CGS	ZERO BIAS G-S JUNCTION CAPACITANCE	0	5PF
7	CGD	ZERO BIAS G-D JUNCTION CAPACITANCE	0	1PF
8	PB	GATE JUNCTION POTENTIAL	1	0.6
9	IS	GATE JUNCTION SATURATION CURRENT	1.0E-14	1.0E-14

----- MOSFET MODELS (BOTH N AND P CHANNELS)

THE MOSFET MODEL IS ALSO DERIVED FROM THE FET MODEL OF SHICHMAN AND HODGES. THE DC CHARACTERISTICS OF THE MOSFET ARE DEFINED BY THE PARAMETERS VTO, BETA, AND LAMBDA, WHICH ARE IDENTICAL TO THE PARAMETERS FOR THE JFET, PHI AND GAMMA, WHICH DETERMINE THE VARIATION OF THRESHOLD VOLTAGE WITH SUBSTRATE VOLTAGE, AND IS, THE SATURATION CURRENT OF THE TWO SUBSTRATE JUNCTIONS. CHARGE STORAGE IS MODELED BY THREE CONSTANT CAPACITORS, CGS, CGD, AND CGB, AND NONLINEAR DEPLETION LAYER CAPACITANCES FOR BOTH SUBSTRATE JUNCTIONS WHICH VARY AS THE -1/2 POWER OF JUNCTION VOLTAGE AND ARE DETERMINED BY THE PARAMETERS CBD, CBS, AND PB.

	NAME	PARAMETER	DEFAULT	TYPICAL
1	VTO	THRESHOLD VOLTAGE	2.0	2.0
2	PHI	SURFACE POTENTIAL	0.5	0.7
3	BETA	TRANSCONDUCTANCE PARAMETER	1.0E-4	1.0E-6
4	GAMMA	BULK THRESHOLD PARAMETER	0	1.0
5	LAMBDA	CHANNEL LENGTH MODULATION PARAMETER	0	0.1
6	RD	DRAIN OHMIC RESISTANCE	0	100
7	RS	SOURCE OHMIC RESISTANCE	0	100
8	CGS	GATE-SOURCE CAPACITANCE	0	0.01PF
9	CGD	GATE-DRAIN CAPACITANCE	0	0.01PF
10	CGB	GATE-BULK CAPACITANCE	0	0.01PF
11	CBD	ZERO BIAS B-D JUNCTION CAPACITANCE	0	0.01PF
12	CBS	ZERO BIAS B-S JUNCTION CAPACITANCE	0	0.01PF
13	PB	BULK JUNCTION POTENTIAL	1	0.7
14	IS	BULK JUNCTION SATURATION CURRENT	1.0E-14	1.0E-14

CONTROL CARDS

***** TITLE CARD

EXAMPLE OP AMP CIRCUIT JOE J STUDENT EECS 241

THIS CARD MUST BE THE FIRST CARD IN THE INPUT DECK. ITS CONTENTS ARE PRINTED VERBATIM AS THE HEADING FOR EACH SECTION OF OUTPUT.

***** .END CARD

GENERAL FORM .END

THIS CARD MUST ALWAYS BE THE LAST CARD IN THE INPUT DECK. NOTE THAT THE PERIOD IS AN INTEGRAL PART OF THE NAME. IF THE .END CARD IS OMITTED, THE NEXT JOB WILL BE READ IN AS PART OF THE JOB MISSING THE .END CARD, AND NEITHER JOB WILL BE RUN SUCCESSFULLY.

***** COMMENT CARD

GENERAL FORM * ANY COMMENTS

EXAMPLE * RF=1K GAIN SHOULD BE 100

THIS CARD IS PRINTED OUT IN THE INPUT LISTING BUT IS OTHERWISE IGNORED.

***** NO PRINT CARD

GENERAL FORM .NP

THIS CARD SUPPRESSES THE SUMMARY OF INPUT DATA THAT IS NORMALLY PRINTED AFTER READING THE INPUT DECK. IT DOES NOT SUPPRESS THE LISTING OF THE INPUT DECK OR ANY ERROR MESSAGES THAT MAY OCCUR.

***** .TEMP CARD

GENERAL FORM .TEMP TE1 TE2 ...

EXAMPLE .TEMP -55.0 25.0 125.0

THIS CARD SPECIFIES THE TEMPERATURES AT WHICH THE CIRCUIT IS TO BE SIMULATED. TE1, TE2, ... ARE THE DIFFERENT TEMPERATURES, IN DEGREES C. A MAXIMUM OF FIVE TEMPERATURES ARE ALLOWED. TEMPERATURES LESS THAN -223.0 DEG C ARE IGNORED.

***** .OUTPUT CARD

GENERAL FORM
```
.OUTPUT VXXXXXX   N+   N-
.OUTPUT IXXXXXX VYYYYYY
.OUTPUT NOISE
```

EXAMPLES
```
.OUTPUT VMIXER 13 27
.OUTPUT IBASE1 V17
```

THIS CARD DEFINES AN OUTPUT VARIABLE. FOR VOLTAGE OUTPUTS, THE NAME MUST BEGIN WITH A V, AND N+ AND N- ARE THE POSITIVE AND NEGATIVE NODE OF THE OUTPUT VOLTAGE. FOR CURRENT OUTPUTS, THE OUTPUT NAME MUST BEGIN WITH AN I, AND VYYYYYY IS THE NAME OF THE INDEPENDENT VOLTAGE SOURCE THAT THE CURRENT IS FLOWING IN. POSITIVE CURRENT FLOWS FROM THE POSITIVE NODE, THROUGH THE SOURCE, TO THE NEGATIVE NODE. THE OUTPUT VARIABLE NAME NOISE IS RESERVED FOR THE NOISE ANALYSIS, AND THE OUTPUT NOISE AND EQUIVALENT INPUT NOISE CAN BE PRINTED AND PLOTTED IN THE SAME FASHION AS OTHER OUTPUT VARIABLES.

OUTPUTS CAN BE PRINTED IN TABULAR FORM OR PLOTTED AS LINE PRINTER PLOTS. THERE ARE EIGHT DIFFERENT OPTIONS WHICH CAN BE PRINTED AND/OR PLOTTED:

DC	DC TRANSFER CURVE OUTPUT
TR	TRANSIENT ANALYSIS OUTPUT
RE	AC ANALYSIS OUTPUT, REAL PART
IM	AC ANALYSIS OUTPUT, IMAGINARY PART
MA	AC ANALYSIS OUTPUT, MAGNITUDE
PH	AC ANALYSIS OUTPUT, PHASE
OU	NOISE ANALYSIS OUTPUT, TOTAL OUTPUT NOISE VOLTAGE
IN	NOISE ANALYSIS OUTPUT, EQUIVALENT INPUT NOISE

AN OUTPUT CAN BE PRINTED OR PLOTTED BY APPENDING THE LETTERS PRINT OR PLOT, FOLLOWED BY ANY COMBINATION OF THE EIGHT OUTPUT OPTIONS, TO THE .OUTPUT CARD:

EXAMPLES
```
.OUTPUT V13 13 0 PRINT MA DC TR
.OUTPUT IIN VIN PRINT PH RE DC
.OUTPUT VOUT 17 2 PLOT MA TR PRINT DC
.OUTPUT I13 V13 PLOT PH DC
.OUTPUT VTHREE 3 0 PRINT DC PLOT TRAN
.OUTPUT NOISE PRINT IN PLOT OU
```

THE PROGRAM WILL AUTOMATICALLY DETERMINE THE MINIMUM AND MAXIMUM VALUES OF THE OUTPUT VARIABLE AND SCALE THE PLOT TO FIT THESE LIMITS. THE AUTOMATIC SCALING FEATURE CAN BE OVERIDDEN BY SPECIFYING PLOT LIMITS AFTER THE OUTPUT OPTION. THE PLOT LIMITS APPLY ONLY TO THE OPTION THAT THEY FOLLOW.

EXAMPLE
```
.OUTPUT V12 12 0 PLOT MA PH -20 30 TR 0 5
```

IN THIS EXAMPLE, THE PROGRAM WILL DETERMINE LIMITS FOR THE MAGNITUDE PLOT, BUT WILL PLOT THE PHASE BETWEEN -20 DEGREES AND 30 DEGREES, AND WILL PLOT THE TRANSIENT RESPONSE BETWEEN 0 VOLTS AND 5 VOLTS.

***** .DC CARD

GENERAL FORM .DC OP OUTPUT INPUT TC ELNAME VSTART VSTOP VINCR

EXAMPLES
```
.DC OP
.DC TC VIN 0 5 0.5
.DC OP VOUT VIN TC VIN 0 5 0.5
```

FOR THE SMALL SIGNAL TRANSFER FUNCTION, OUTPUT IS THE OUTPUT VARIABLE AND INPUT IS THE INPUT SOURCE. THE PROGRAM WILL COMPUTE THE DC SMALL SIGNAL VALUE OF THE TRANSFER FUNCTION (OUTPUT/INPUT), INPUT IMPEDANCE, AND OUTPUT IMPEDANCE. IF THE TRANSFER FUNCTION VALUE IS NOT DESIRED, OMIT THE OUTPUT AND INPUT SPECIFICATIONS. IF THE DC OPERATING POINT IS NOT DESIRED, OMIT THE LETTERS OP. HOWEVER, A DC OPERATING POINT WILL ALWAYS BE COMPUTED PRIOR TO AN AC SMALL SIGNAL ANALYSIS OR A TRANSIENT ANALYSIS.

FOR TRANSFER CURVES, ELNAME IS THE NAME OF THE VARIABLE SOURCE, VSTART IS THE STARTING SOURCE VALUE, VSTOP IS THE FINAL SOURCE VALUE, AND VINCR IS THE INCREMENT. THE TOTAL NUMBER OF POINTS TO BE COMPUTED CANNOT EXCEED 101. IF A TRANSFER CURVE IS NOT DESIRED, OMIT THE LETTERS TC AND THE TRANSFER CURVE PARAMETERS.

***** .AC CARD

GENERAL FORM
```
.AC DEC ND FSTART FSTOP NOISE OUTPUT INPUT NUMS
.AC OCT NO FSTART FSTOP NOISE OUTPUT INPUT NUMS
.AC LIN NP FSTART FSTOP NOISE OUTPUT INPUT NUMS
```

EXAMPLES
```
.AC DEC 10 1 10KHZ
.AC DEC 20 1 100KHZ NOISE VOUT VIN 10
.AC DEC 10 1 100MEG NOISE VOUT V21
```

DEC STANDS FOR DECADE VARIATION, AND ND IS THE NUMBER OF POINTS PER DECADE. OCT STANDS FOR OCTAVE VARIATION, AND NO IS THE NUMBER OF POINTS PER OCTAVE. LIN STANDS FOR LINEAR, AND NP IS THE NUMBER OF POINTS. FSTART IS THE STARTING FREQUENCY, AND FSTOP IS THE FINAL FREQUENCY. THE TOTAL NUMBER OF FREQUENCY POINTS TO BE COMPUTED CANNOT EXCEED 101.

FOR NOISE ANALYSIS, OUTPUT IS THE NAME OF A VOLTAGE OUTPUT VARIABLE. THIS OUTPUT, WHICH MUST BE A VOLTAGE, WILL BE USED AS THE SUMMING POINT. INPUT IS THE NAME OF AN INDEPENDENT VOLTAGE OR CURRENT SOURCE. THE TOTAL OUTPUT NOISE IS DIVIDED BY THE TRANSFER FUNCTION (OUTPUT/INPUT) TO OBTAIN THE EQUIVALENT INPUT NOISE LEVEL. NUMS IS THE SUMMARY INTERVAL. AT EVERY NUMS FREQUENCY POINTS, THE INDIVIDUAL CONTRIBUTIONS OF EACH ELEMENT ARE PRINTED OUT. IF NUMS IS OMITTED OR SET TO ZERO, NO SUMMARY PRINTOUT WILL OCCUR. FOR REASONS OF REDUCING PRINTOUT, NUMS SHOULD BE AS LARGE AS POSSIBLE. IF THE NOISE ANALYSIS IS NOT DESIRED, OMIT THE LETTERS NOISE AND THE NOISE ANALYSIS SPECIFICATIONS.

***** .TRAN CARD

GENERAL FORM .TRAN TSTEP TSTOP TSTART FOUR OUTPUT FREQ

EXAMPLES .TRAN 1NS 100NS
.TRAN 1NS 1000NS 500NS
.TRAN 1NS 100NS FOUR VOUT 100MEG

TSTEP IS THE PRINTING INCREMENT BETWEEN TIMEPOINTS, TSTOP IS THE FINAL TIMEPOINT, AND TSTART IS THE INITIAL TIMEPOINT. IF TSTART IS OMITTED, IT IS ASSUMED TO BE ZERO. THE TRANSIENT ANALYSIS ALWAYS BEGINS AT TIME ZERO. IN THE INTERVAL (ZERO, TSTART), THE CIRCUIT IS ANALYZED (TO REACH A STEADY STATE), BUT NO OUTPUTS ARE STORED. IN THE INTERVAL (TSTART, TSTOP), THE CIRCUIT IS ANALYZED AND OUTPUTS ARE STORED. THE NUMBER OF TIMEPOINTS IN THE INTERVAL (ZERO, TSTOP) CANNOT EXCEED 1001, AND THE NUMBER OF TIMEPOINTS IN THE INTERVAL (TSTART, TSTOP) CANNOT EXCEED 101.

FOR FOURIER ANALYSIS, OUTPUT IS THE OUTPUT VARIABLE AND FREQ IS THE FUNDAMENTAL FREQUENCY. THE FOURIER ANALYSIS IS PERFORMED OVER THE INTERVAL (TSTOP-PERIOD,TSTOP), WHERE TSTOP IS THE FINAL TIME SPECIFIED, AND PERIOD IS ONE PERIOD OF THE FUNDAMENTAL FREQUENCY. THE DC COMPONENT AND THE FIRST NINE COMPONENTS ARE DETERMINED. FOR MAXIMUM ACCURACY, THE NUMBER OF PERIODS IN THE INTERVAL (TSTART,TSTOP) SHOULD BE AS SMALL AS POSSIBLE (BUT NEVER LESS THAN ONE). THIS INSURES THAT THE NUMBER OF TIMEPOINTS IN ONE FUNDAMENTAL IS AS LARGE AS POSSIBLE. IF THE FOURIER ANALYSIS IS NOT DESIRED, OMIT THE LETTERS FOUR AND THE FOURIER SPECIFICATIONS.

FOR SOME PROBLEMS, TO AVOID NUMERICAL INSTABILITY IN THE INTEGRATION ALGORITHM, IT MAY BE NECESSARY TO SPECIFY AN INTERNAL TIME STEP WHICH IS SMALLER THAN THE PRINTING INCREMENT (TSTEP). EXAMPLES OF THIS TYPE OF PROBLEM ARE ASTABLE MULTIVIBRATORS, SWEEP CIRCUITS, AND OTHER HIGHLY NONLINEAR CIRCUITS WHICH HAVE WIDELY SEPARATED TIME CONSTANTS. SPICE ALLOWS THE USER TO SEGMENT THE TIME INTERVAL INTO FROM ONE TO FIVE SUBINTERVALS AND SPECIFY A DIFFERENT TIME STEP FOR EACH SUBINTERVAL. THE INTERNAL TIME STEPS AND SUBINTERVAL ENDPOINTS ARE SPECIFIED AFTER THE STARTING TIME (TSTART) AND BEFORE THE FOURIER ANALYSIS OPTIONS:

GENERAL FORM .TRAN TSTEP TSTOP TSTART D1 E1 D2 E2 ... D5 E5 FOUR OUTPUT FREQ

EXAMPLE .TRAN 1NS 100NS 0 0.1NS 10NS 0.5NS 100NS

D1 IS THE FIRST INTERNAL TIMESTEP AND E1 IS THE ENDPOINT OF THE FIRST SUBINTERVAL, D2 IS THE SECOND INTERNAL TIMESTEP AND E2 IS THE ENDPOINT OF THE SECOND SUBINTERVAL, AND SO ON. IN THIS EXAMPLE, THE PROGRAM WILL USE AN INTERNAL TIME STEP OF 0.1NS FOR THE INTERVAL (0,10NS) AND AN INTERNAL TIME STEP OF 0.5NS FOR THE INTERVAL (10NS,100NS). OUTPUT IS STILL STORED EVERY 1NS. THE TOTAL NUMBER OF TIMEPOINTS TO BE COMPUTED CANNOT EXCEED 1001.

EXAMPLE .TRAN 1US 100US 0 0.1US 100US

IN THIS EXAMPLE, THE PROGRAM WILL USE AN INTERNAL TIME STEP OF 0.1US OVER THE ENTIRE TRANSIENT INTERVAL BUT WILL STORE OUTPUT ONLY AT 1US INTERVALS. HENCE, THE PROGRAM STORES AND OUTPUTS EVERY TENTH TIMEPOINT.

EXAMPLE DATA DECKS

THE FOLLOWING DECK DETERMINES THE DC OPERATING POINT AND SMALL SIGNAL TRANSFER FUNCTION OF A SIMPLE DIFFERENTIAL PAIR.

```
SIMPLE DIFFERENTIAL PAIR
VCC 7 0 DC 12
VEE 8 0 DC -12
VIN 1 0
RS1 1 2 1K
RS2 6 0 1K
Q1 3 2 4 MOD1
Q2 5 6 4 MOD1
RC1 7 3 10K
RC2 7 5 10K
RE 4 8 10K
.MODEL MOD1 NPN BF=90 VA=50 IS=1.0E-12 RB=100
.OUT VOUT 5 0
.DC OP VOUT VIN
.END
```

THE FOLLOWING DECK DETERMINES THE DC TRANSFER CURVE AND THE TRANSIENT PULSE RESPONSE OF A SIMPLE RTL INVERTER. THE INPUT IS A PULSE FROM 0 TO 5 VOLTS WITH DELAY, RISE, AND FALL TIMES OF 2NS AND A PULSE WIDTH OF 30NS. THE TRANSIENT INTERVAL IS 0 TO 100NS IN 1NS STEPS.

```
SIMPLE RTL INVERTER
VCC 4 0 DC 5
VIN 1 0 PULSE 0 5 2NS 2NS 2NS 30NS
RB 1 2 10K
Q1 3 2 0 Q1
RC 4 5 1K
.OUTPUT VC 3 0 PRINT DC PLOT TR 0 5
.MODEL Q1 NPN BF=20 RB=100 TF=0.1NS CJC=2PF
.DC TC VIN 0 5 0.1
.TRAN 1NS 100NS
.END
```

THE FOLLOWING DECK DETERMINES THE AC SMALL SIGNAL RESPONSE OF A ONE TRANSISTOR AMPLIFIER OVER THE FREQUENCY RANGE OF 1HZ TO 100MEGHZ.

```
ONE TRANSISTOR AMPLIFIER
VCC 5 0 DC 12
VEE 6 0 DC -12
VIN 1 0 AC 1
RS 1 2 1K
Q1 3 2 4 X33
RC 5 3 500
RE 4 6 1K
CBYPASS 4 0 1UFD
.OUT V3 3 0 PLOT MA PH
.AC DEC 10 1HZ 100MEGHZ
.MODEL X33 NPN BF=30 RB=50 VA=20
.END
```