Radiation Effects and Hardening of MOS Technology: Devices and Circuits

H. L. Hughes and J. M. Benedetto

Abstract—**Total ionizing dose radiation effects on the electrical properties of metal-oxide-semiconductor devices and integrated circuits are complex in nature and have changed much during decades of device evolution. These effects are caused by radiation-induced charge buildup in oxide and interfacial regions. This paper presents an overview of these radiation-induced effects, their dependencies, and the many different approaches to their mitigation.**

Index Terms—**Aerospace testing, CMOS integrated circuits, hydrogen, magnetic resonance, MOS devices, power MOSFETs, radiation effects, radiation hardening.**

I. Introduction

In addition to providing an overview of the field during the past 40 years, this paper can serve as a guide to locate literature in a wide range of topics related to total ionizing dose (TID) radiation effects and hardening of bulk metal-oxide-semiconductor (MOS) devices and integrated circuits (ICs). TID effects referenced here are due to accumulation of ionizing radiation over time, which results in long-term degradation in device performance. (Single event and transient ionization radiation effects, as well as displacement effects, are covered elsewhere in this journal issue.)

A short background section introduces some terminology and basic concepts. This is followed by a brief chronology and a discussion of various radiation-induced effects on the electrical properties of MOS transistors and integrated circuits. The later sections of this paper discuss factors influencing MOS TID radiation sensitivity and conclude with techniques and approaches for hardening that have been published previously in the open literature.

Much of the hardening of MOS technology has been based on phenomenological results from experiments performed at various times along the evolutionary path of MOS technology. These technology-specific experimental results, as well as recent efforts to build in and predict hardness from first-principles atomic models [such as those utilizing electron spin resonance (ESR)] [1], [2] are reviewed. There is no single "magic" ingredient or process available to produce radiation hardened ICs. Radiation hardness is determined by complex interrelationships among technology, design, and fabrication procedures, as well as by the specific radiation environments [3]. Explanations of many different factors and complex interrelationships that affect the radiation responses of MOS devices and integrated circuits are brief in order to cover a wide range of material and topics. The primary purpose of this paper is to provide a resource to help locate detailed explanations about the various mechanisms, effects, and techniques published in the refereed literature.

II. Background

As the linchpin of integrated circuits, MOS structures are crucial elements in most silicon device technologies, including digital complementary-metal-oxide-semiconductor (CMOS), N-channel (NMOS), and P-channel (PMOS) ICs, as well as linear CMOS and bipolar CMOS (BICMOS) ICs, charge coupled devices (CCDs), power MOS field effect transistors (MOSFETs), and nonvolatile memories. CMOS integrated circuit technology alone has dominated the electronics industry for more than 30 years, channel size scaling in length by a factor of over 100 in size during this time period. Changes associated with the evolution to smaller and smaller devices have had a dramatic influence on the radiation effects and hardening procedures of MOS-based structures. Updated alterations in fabrication processing, design and layout procedures all require continued modification to accommodate further scaling [4]. Requirements of scaling for either high performance or low power purposes are different and thus have a different impact on TID hardness. The evolution of IC density requires that device geometries scale proportionately, impacting MOS radiation hardness, depending on whether power or performance is the overriding design goal [5]. Not only is the geometry changing from one device generation to the next, but also the processing techniques, materials, and processing tools are changing. It is now fairly well known that TID radiation effects are all influenced, in varying degrees, by each of these factors from one generation to the next.

TID radiation effects in MOS devices occur in the relatively thin noncrystalline dielectric films and at the dielectric film/silicon interfaces. These dielectric films (typically SiO_2) range in thickness from 2 nm (for modern gate oxides) to 1000 nm (for field oxides) and are used throughout MOS IC structures for purposes such as gate control, electrical isolation (lateral isolation using field oxides, vertical isolation using buried oxides and intermetallic isolation, including the use of low k dielectrics), passivation layers (e.g., P-glass and silicon nitride), and spacers, such as in lightly doped-drain (LLD) processes. Simply described, device degradation is caused by radiation-induced charge buildup in these thin film dielectric regions and

Manuscript received April 7, 2003. This work was supported by the Defense Threat Reduction Agency (DTRA) through the Radiation Hardened Microelectronics Program.

H. L. Hughes is with the U.S. Naval Research Laboratory, Washington, DC 20375 USA (e-mail: hughes@estd.nrl.navy.mil).

J. M. Benedetto is with MRC Microelectronics, Colorado Springs, CO 80919 USA (e-mail: benedetto@mrcmicroe.com).

Digital Object Identifier 10.1109/TNS.2003.812928

0018-9499/03$17.00 © 2003 IEEE

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

interfaces; however, the details related to the basic mechanisms of radiation effects in MOS devices are very complicated [6]. (For basic mechanisms details see the review paper by Oldham and McLean in this journal.)

Due to the aforementioned complexities MOS TID radiation sensitivity depends on many factors involving details of design and fabrication, as well as conditions of use and radiation exposure. In particular, TID radiation-induced charge buildup in MOS devices depends on: dose, dose-rate, and type of ionizing radiation [7]–[9], applied and internal electric fields (including space-charge effects) [10], [11], device geometry [12], [13], [5], [14], operating temperature [15], [16], postirradiation conditions (e.g., time and temperature) [17], [18], dielectric material properties (stoichiometry, structure, defects, and doping) [19], [20], fabrication processing (oxide growth and anneal conditions), oxide impurities (including hydrogen [21]–[23], nitrogen, [24], [25], and sodium [26], [27]), final packaging processes [28], [29], burn-in [30] reliability screens [31], and aging [32]. In addition, issues of IC architecture also impact survivability against TID effects [33].

III. Chronology

A. 1960–1969

The radiation sensitivity of MOS devices was discovered in the early 1960s at the Naval Research Laboratory (NRL) [34]. Previously, it was thought that newly introduced MOS transistors (being majority-carrier devices) would not be as radiation sensitive as bipolar transistors and, as such, would be attractive devices for space applications. The high input impedance, low current attributes of MOS devices [35] were being explored at that time by NRL for use in the world's first reconnaissance satellite (GRABE), which was intended to fill the void left when the USA's U-2 flight was shot down by the U.S.S.R. in May 1960. Prior NRL efforts had been directed at the basic mechanisms of radiation-induced surface effects using cobalt-60 gamma rays to investigate the effects of ionizing radiation on oxide passivated bipolar transistors [36].

The early NRL work determined that the fundamental cause of damage in devices with oxide regions was related to charge buildup *in* the oxide and not due to the usual radiation-induced ionic effects *on* device surfaces (as was the case for the unpassivated bipolar transistors that failed in the Telstar satellite exposed to radiation from the high altitude nuclear test, Starfish) [37]. The newly found debilitating effect of radiation-induced charge buildup in the gate oxides of MOS transistors using cobalt-60 gamma rays was confirmed by other groups and with other types of radiation, including: flash X-rays, TRIGA reactor radiation, and high energy electrons, both pulsed and steady state [38]–[42]. These efforts established that the dominant radiation effects in MOS devices were due to TID effects, and not due to displacement damage, the usual cause of radiation-induced degradation in bipolar devices.

In order to gain insight into what types of radiation-induced centers were being generated, and going beyond electrical measurements of TID effects, electron spin resonance (ESR) was explored. (ESR can detect point defects in dielectric films by sensing unpaired spins, thus the detection is charge state dependent.) The first ESR, also referred to as electron paramagnetic resonance (EPR), measurements on irradiated MOS structures were performed in the late 1960s at the RCA Sarnoff Laboratories [43]. It was found that oxide/silicon structures (formed by a dry oxygen growth with a post oxidation heat treatment in hydrogen at 1100 °C for 10 min and irradiated with 1×10^{17} electrons/cm^2) generated 2×10^{12} EPR centers/cm^2. The controls with no postoxidation heat treatment, as well as samples heat-treated in helium, showed no increase in EPR centers [43]. This work initiated concern about high temperature hydrogen heat treatments and helped to stimulate radiation hardening of the RCA process by changing from forming gas anneals $(N_2 + H_2)$ to 100% nitrogen anneals (helium being too expensive). This process change eventually enabled, a decade later, the production of CMOS parts able to survive the radiation environments related to a Jupiter space mission.

The Defense Atomic Support Agency (DASA) and U.S. Air Force sponsored programs to investigate ways to further harden MOS transistors. DASA supported programs at Hughes Aircraft Co. (HAC) and Autonetics [later, Rockwell International (RI)] to modify the gate dielectric materials through doping, as well as by growth and anneal conditions [44]–[46].

During this decade, the Air Force pursued aluminum oxide at RCA as an alternative dielectric material [47], [48]. Although this approach looked promising from a TID standpoint, it was never put into production because of process-related instability problems [49]. However, more than 20 years after these initial attempts, use of deposited aluminum oxide is again of interest as a high-k (high dielectric constant) alternative to ultra-thin thermally grown silicon dioxide [50], [51].

B. 1970–1979

During the early 1970s, the Defense Nuclear Agency (DNA, formerly DASA) established a major program to develop radiation hardened CMOS integrated circuits. Previously, MOS ICs were limited to the use of P-channel type MOS devices because N-channel MOS (which operates with positive gate biases) exhibited instabilities due to positive ions (primarily sodium) contaminating the gate oxide. The Na^+ ion contamination in the gate oxides of N-channel MOS transistors would drift to the silicon/silicon dioxide interface under the operational positive gate bias and cause changes in device characteristics. CMOS (which uses both N- and P- channel transistors) became possible with the enhanced capability to produce stable sodium-free oxides [52]. This capability enabled low-power CMOS technology to dominate digital electronics for the next three decades, when the channel length evolved down in size 100-fold from an initial value of 18 to less than 0.18 μm (and still is progressing to smaller values at this time).

Using ESR (beyond the initial RCA work related to postoxidation anneal ambients), it was shown at NRL that the oxides of irradiated MOS structures produce an ESR signal (called an E' center) [53] identical to that observed in irradiated bulk glass (silica) [54], [55] and modeled by Lehigh University workers as an oxygen vacancy in the structural network of glass [56]. The ESR signal found by NRL in thin TID irradiated MOS silicon dioxide films, coupled with the Lehigh work, led to a

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

damage mechanism possibly being related to oxygen deficiency defects in the oxide. Agreement with the bias dependency of radiation-induced oxide charge was observed in that a positive gate bias during irradiation caused a $10\times$ enhancement of the E' signal. Etch-back studies at NRL found that most of the radiation-induced centers were located near the silicon dioxide/silicon interface. This work pointed the way to the possibility of controlling oxidation growth parameters for hardening purposes.

In light of this new finding, the question arose as to whether or not alternative gate oxide approaches were still necessary for hardening. DNA then sponsored a competitive runoff of three alternative hardened gate oxide approaches, versus controlled thermally grown silicon dioxide. Metal-gate CMOS inverter circuits, called CD4007s, were fabricated using different hardened gate oxides [57]–[60], and undoped silicon dioxide, at RCA-Somerville and HAC [49], [59]. An unexpected result from these multisupplier comparisons was that undoped silicon dioxide—if grown under improved, controlled conditions—could be made sufficiently radiation hard to meet most system requirements [59], [61]–[63].

Consequently, it was discovered that metal gate small-scale integrated (SSI) CMOS logic circuits could be made megarad-hard if the following controlled processing procedures were followed: gate oxides were grown in dry oxygen at 1000 °C [19], [64], [59], [24]; furnaces were cleaned by a flowing HCl purge [59], [61]; postoxidation anneals were done in nitrogen at 850 °C to 900 °C (reduced in temperature from the standard anneal which usually was performed at the oxide growth temperature to reduce initial fixed charge) [62]; and metallization was deposited by a nonradiative process, such as using inductively heated crucibles (no electron beam nor sputtering type sources could be used) [64]. The thicknesses (t) of oxide regions were minimized based on the strong power-law relationship (t^3) of radiation-induced threshold voltage shift on oxide thickness [65].

To avoid field oxide TID effects, the layout had to be changed so that the gate oxide was patterned to extend to the guardband lateral isolation region (no thick field oxide was allowed inside the p-n junction type guardband) [66], [67]. National Semiconductor Corporation (NSC), RCA, and later Harris Semiconductor offered megarad-hard CMOS metal gate ICs fabricated using the aforementioned modified processing of silicon dioxide gate dielectric material. For SOS ICs the preferred oxide growth was a lower temperature wet oxide growth (850 °C to 900 °C) to avoid high temperature perturbations of the silicon/sapphire interface causing unwanted back-channel leakage current [68]–[71].

In order to support higher density ICs, lateral device-to-device electrical isolation had to be changed from p-n junction guardband type structures to smaller oxide regions. As a result, this change toward the use of field oxides introduced a new TID oxide-related vulnerability. For more dense constrained designs, a hardened field oxide was necessary. Sandia National Laboratory (SNL) developed an early type of radiation-hard field oxide, called direct-moat, for application to nonguardbanded IC designs and successfully demonstrated performance and hardness on a 1 Kb CMOS SRAM [72]. This technique was extended and put into production by Harris [73].

As a result of these successful hardening efforts, TID hardened metal-gate CMOS was used in various space programs, including DMSP, TIROS, DSP, and GPS, as well as in the Voyager and Galileo space probes.

C. 1980–1989

In the 1980s, the primary emphasis was placed on hardening silicon-gate CMOS ICs, including those in the Department of Defense (DoD) Very High Speed Integrated Circuit (VHSIC) Program. Hardening efforts on VHSIC 1.25 μm silicon-gate technology were carried out on the following MOS technologies: CMOS/ silicon-on-sapphire (SOS), NMOS, and bulk CMOS. It was found that hardening of high density, silicon-gate technology was significantly more complex than hardening the previous generations of aluminum-gate ICs. With silicon-gate MOS ICs, design, as well as layout issues became part of the hardening equation.

To meet increasing demand for hardened ICs of greater device density, a hardened field oxide structure smaller than the aforementioned SNL direct-moat type was necessary. The semiconductor industry pursued various new lateral oxide isolation approaches, such as local oxidation of silicon (LOCOS), poly-buffered LOCOS, and selected poly-Si oxidation (SEPOX), each having hardening advantages and disadvantages. Of major concern to the IC builder is the extent of oxide encroachment, such as the LOCOS "bird's beak," that reduces active device area and causes increased radiation sensitivity due to the stressed nature of the oxide [74]. Double-layer deposited oxide structures using dopants such as boron and phosphorus for hardening were introduced [75], [76]. TID effects in deposited field oxides studied by ESR were found to be fundamentally different from thermal oxides, and it was found that E' centers could not be generated by hole trapping, as in thermal oxides [77].

Further insights into the role of oxide processing on TID effects were provided by ESR studies during the 1980s. ESR differences were observed due to process related effects for rad-hard and rad-soft thermally grown oxides [78]. Reassuringly, similar process dependencies, such as for wet versus dry treatments, were found for bulk amorphous silicon dioxide materials [79]. SNL quantitatively correlated radiation-induced, trapped positive oxide-charge in MOS structures to E' centers [80], [81]. The SNL workers correlated radiation-induced interface states (defined as electronic levels located spatially at the dielectric/silicon interface and energetically within the band gap of the active silicon) with ESR signals called P_b centers. (See Section IV-A7c for details related to interface states.) They found this correlation with cobalt-60 gamma-ray irradiated MOS structures on $\langle 111\rangle$ silicon, without electrical-bias during irradiation [82], [80]. Also, it was found for $\langle 111\rangle$ silicon that both the interface states and P_b centers annealed out within the same temperature range, 100 °C to 250 °C [83]. Furthermore, both were annealed out when a positive electrical bias was applied to the gate [84], [81]. ESR studies were

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

extended to oxides grown on ⟨100⟩ silicon (the orientation used for CMOS integrated circuits) by the group at Pennsylvania State University (PSU). For cobalt-60 gamma-ray irradiated (with positive gate bias) oxides grown on ⟨100⟩ silicon, two P_b type centers were generated, the $P_{\rm bo}$ and P_{b1}, where $P_{\rm bo}$ is chemically the same as the P_b center in ⟨111⟩. Irradiation caused greater increases in the $P_{\rm bo}$ than the P_{b1} [85]. It was imperative that processes be determined to minimize all of the above radiation-induced P_b centers in order to reduce the damaging effects of radiation-induced interface states ($N_{\rm it}$).

In order to develop processes to radiation harden CMOS devices and circuits, it is necessary to reduce radiation-induced oxide trapped charge ($N_{\rm ot}$), as well as $N_{\rm it}$. Based on insights gleaned from ESR, it became apparent that processes to reduce both radiation induced E' and P_b centers needed to be developed. Since many unit processes needed to be evaluated, and quick-turn-around was necessary to complete the fabrication schedule, an alternative to ESR was established (ESR being a research tool, not available on-line within semiconductor facilities). A table top X-ray irradiator, the ARACOR 4100, was used extensively to evaluate experimental radiation hardened processes [86]. Electrical device parameters (see Section IV) versus radiation dose, provided by the ARACOR, were used to qualify various unit processes.

D. 1990–1999

In the 1990s, the emphasis in hardening digital ICs was on submicron (gate-length) silicon-gate CMOS technologies at Honeywell, Lockheed-Martin, United Technology Microelectronics Center (UTMC), NSC, and Texas Instruments (TI). The gate oxide became intrinsically hard to TID because of its reduced thickness (due to the power-law mentioned in Section III-B.). Work in the 1980s had shown that (due to tunnel currents) the gate oxide radiation problem would vanish once the gate oxide thickness fell below 10 nm [87]. This, indeed, has happened. The first commercial production of oxides with thicknesses less than 10 nm were manufactured in the 1990s. For bulk CMOS, the main hardening issue then became the field oxide lateral isolation structures, which needed to be scaled to even smaller geometries. To meet the scaling requirements, shallow trench isolation (STI) approaches, with no bird's beak encroachment, were commonly used near the end of the decade. See Figs. 1 and 2 for a comparison of LOCOS and STI structures and their corresponding yield as a function of channel length. Fig. 1 shows how the effective channel width ($W_{\rm eff}$) is reduced by the "bird's beak" inherent to LOCOS. As it can be seen from Fig. 2, due to yield problems, LOCOS lateral isolation needed to be abandoned for device geometries scaled below 0.4 μm [88].

Interestingly, there is a wide variation in the intrinsic hardness of STI. In some cases, TID failure levels for STI were observed at <10 krad (SiO_2) [89] while in other cases radiation hardness levels of greater than 100 krad(Si) were measured on some commercial technology. It is understood that the hardness of the STI region depends on a number of features, including geometry and type of trench refill oxide. ESR studies of trench refill oxides found that doped phosphor-silicate-glass (PSG) and deposited (TEOS) oxides had radiation-induced charge trapped in phosphorus and carbon related ESR centers as well as in E' centers [90].

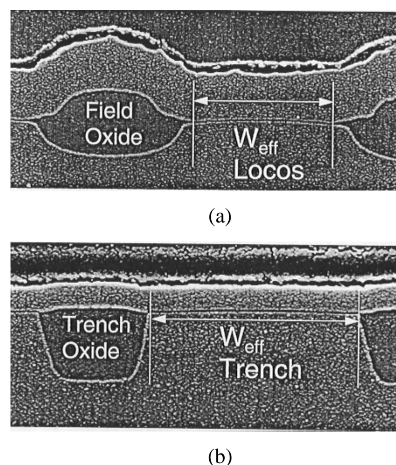

Fig. 1. Transmission electron micrograph (TEM) images of (a) LOCOS and (b) Trench regions, showing less encroachment on the channel width ($W_{\rm eff}$) for Trench than LOCOS (courtesy of J. Schlueter of Novellus Systems/SEMATECH).

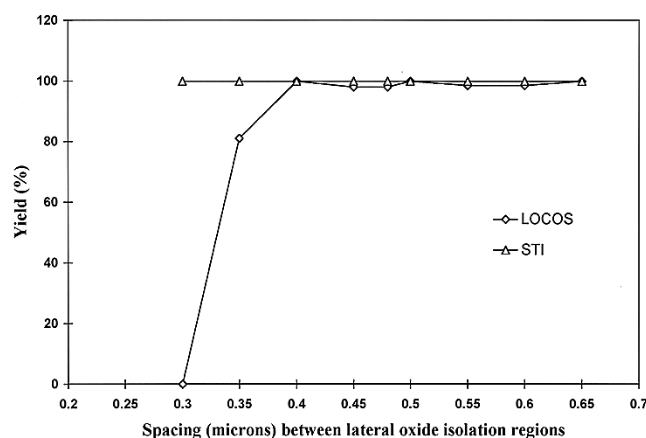

Fig. 2. Yield versus scaling size for LOCOS versus Trench, showing reduced yield for LOCOS for channel scaling below 0.4 μm (courtesy of J. Schlueter of Novellus Systems/SEMATECH).

A hardened STI process was developed by Honeywell and put into production. These hardening efforts produced megarad-hard 1 Mb SRAMs within five years (three technology generations) after the unhardened versions were introduced commercially. UTMC developed a "minimally invasive" process module and was successful at hardening commercial STI to >1 Mrad(Si). Combined with an inherently hardened gate oxide, radiation hardened deep submicron ICs were produced at commercial foundries.

E. 2000 and Beyond

Scaling CMOS channel lengths to 100 nm and smaller requires gate oxide thickness to be less than 4 nm. TID effects on gate threshold voltage are not an issue for digital CMOS technologies while they use ultrathin silicon dioxide films, but this may not be the case for alternative (high k) gate dielectric materials. However, for mixed signal [91] and power MOS ICs [92], where thicker gate oxides are required, radiation-induced

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

threshold voltage shifts are still of concern. Flash memory [93], another MOS technology requiring higher operating voltage and, thus, thicker gate oxides for charge pump circuits, is still very sensitive to TID effects. For example, threshold voltage shifts in charge pump circuits internal to MOS field programmable gate arrays fail at TID levels less than 20 krad (Si) [94].

As CMOS evolves with channel lengths scaled below 0.25 μm, hardening concerns about lateral isolation oxides are still an issue, as well as new alternative high-k gate dielectrics (as discussed in Section V-A2) [95]. Most of the previous approaches for shallow trench hardening are no longer operative for advanced generations of CMOS since they depend on the use of doped glass [96], [97] which cannot be tolerated due to inherent autodoping affecting the thinner films required by scaling constraints. Furthermore, the 1.5 MeV alpha particles created by neutrons reacting with the boron-10 in boron-phosphorous-silicate-glass (BPSG) films cause upsets in submicron devices. Experimental work will be needed to develop hardening processes for undoped trench refill oxides, such as high-density plasma (HDP) and low temperature types.

The new millennium saw the first quantitative data on the role of hydrogen regarding $N_{\rm ot}$. Using ESR and CV measurements on samples with controlled hydrogen doping, it was found that the correlation of E' centers with radiation-induced positive trapped charge depends also on radiolytic hydrogen. Without trapped hydrogen the E' center was found, in this case, to be neutral, and not positively charged, as it had been previously modeled [98]. Thus, the E' center may not account for all of the radiation-induced oxide trapped charge $(N_{\rm ot})$. Previously, it was noted that ionizing radiation, X-rays, and Co-60 gamma rays could cause a hydrogen-related ESR signal to disappear [99], [100]. Hydrogen-related ESR signals, such as the 74 G and 10.2 G doublets, have never been investigated thoroughly enough to provide insight into understanding MOS trapped positive charge effects; heretofore, research focused mainly on the E' center as being due to an oxygen-vacancy related to trapped positive charge $(N_{\rm ot})$. More ESR work needs to be performed from the standpoint of understanding the hydrogen chemistry related to MOS radiation-induced effects and hardening, especially concerning $N_{\rm ot}$.

IV. Radiation-Induced Degradation in the Electrical Properties of MOS Transistors and Integrated Circuits

Radiation-induced oxide and interface trapped charges affect the performance and reliability of MOS transistors and integrated circuits to varying degrees, depending upon a number of operational conditions which are delineated below.

A. Transistor Effects

1) Threshold Voltage Shifts: Threshold voltages for both N- and P-channel MOS transistors shift due to radiation-induced trapped oxide charge $(N_{\rm ot})$ and trapped interface charge $(N_{\rm it})$ (with the caveat that oxides less than 10 nm in thickness show almost no radiation induced threshold voltage shift). The contributions of $N_{\rm ot}$ and $N_{\rm it}$ are additive for P-channels and subtractive for N-channel MOS transistors. Since both types of charge vary with postirradiation time, temperature, and electrical conditions, so does the threshold voltage vary, accordingly.

As an aid in analyzing radiation effects and developing hardening procedures, it is important to determine and control these two components of damage. Radiation-induced oxide charge $N_{\rm ot}$ is the net trapped charge in the bulk of the oxide due to both trapped holes and electrons [101]. Usually $N_{\rm ot}$ is dominated by positive trapped charges and the trapped electrons tend to compensate partially to reduce the net value of $N_{\rm ot}$. However, there are some cases where the $N_{\rm ot}$ is dominated by trapped electrons [102].

Radiation-induced (TID) threshold voltage shifts depend on oxide thickness (t) according to a power-law, t^n, where n can have values of: between one and two [103]–[105], or two [106]–[108], or three [65], depending on processing and electrical biasing effects. Since the majority of results published subsequently have observed the square law usually to be operative (for thermally grown oxides), its use has become routine.

Measured threshold voltage shifts due to irradiation can be separated into these two components using: transistor subthreshold current-voltage characteristics [109], [110], including corrections for dopant deactivation [111] or dual-transistor techniques [112]. These approaches work particularly well on commercial parts since measurements are performed at 2–5 orders of magnitude greater current than subthreshold slope and charge pumping methods [113]–[116]. The dual-transistor approach is not as sensitive to spurious radiation-induced leakage paths such as those due to edge effects. This technique, however, requires that both N- and P-channel transistors be fabricated identically. For example, this would not be the case where buried-channel type P-channel MOS transistors would be used, since they receive a channel implant not used on N-channel transistors. Where this is a problem other methods are available, such as using mobility degradation to determine $N_{\rm it}$ [117], [118]. For instance, the Hall effect has been used to measure the spectral density of postirradiation interface states near the conduction band that affect transconductance degradation due to mobility changes [119].

Partitioning the radiation-induced subthreshold current-voltage characteristics into the oxide $(N_{\rm ot})$ and interface $(N_{\rm it})$ components requires mid-gap neutrality (the contributions of interface states at the mid-gap energy are neutral; i.e., no lateral shift in the CV curve would occur for interface states, implying that interface states above and below the mid-gap energy compensate). For most cases the assumption of mid-gap neutrality is a good engineering approximation, which is usually found to introduce only small errors; however, it should not be used uncritically [120]. For the particular oxides used by SNL, this condition was met [109], [121]. However, for other oxides the condition of mid-gap neutrality was observed not to be satisfied [120], [122].

Saturation of threshold voltage shift at high total dose was modeled with the aid of computer simulation of charge buildup. Saturation was found to be caused by a complex interaction between trap filling and recombination of radiation-generated free electrons with trapped holes, modulated by trapped-hole-distortion of the oxide electric field [123].

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

2) Subthreshold Slope: Radiation-induced subthreshold slope is affected by both trapped interface charge and lateral nonuniformity of trapped oxide charge [113], [124]. Lateral nonuniformity of trapped oxide charge can be caused by a nonuniform deposition of charge or by a nonuniform distribution of traps [125], [126]. These effects degrade device performance by increasing leakage currents.

3) Transconductance: The gain (transconductance) of the MOS transistor is decreased by radiation-induced reduction in carrier mobility in the device channel caused by charges trapped at, or very close to, the silicon/silicon dioxide interface [127]–[132]. Transconductance also can be reduced by increases in surface resistivity such as would be caused in a transistor with LDD regions intended to reduce hot carrier reliability effects. Radiation-induced trapped charge in the spacer oxide, used to fabricate the LLD, has been found to deplete p-type LDDs, increasing the resistivity and causing degradation in transconductance without affecting mobility [133].

4) Channel and Junction Leakage Current and Breakdown: Gate-induced drain leakage (GIDL) current is increased by TID [134], [135]. Trapped charge buildup in lateral oxide isolation regions (field oxide structures) increases transistor edge leakage current [66], [136], [137] and changes junction breakdown voltage (degradation in N-channels and enhancement for P-channel power MOS transistors) [138].

5) Noise: Noise, especially $1/f$ noise, is increased in MOS transistors by TID [22], which also increases noise in power transistors [139]–[141]. The radiation-induced increases in noise have been correlated with oxide-trapped charges [142]–[146] and interface trapped charges [147].

6) Gate Oxide Stability and Breakdown: Ionizing-radiation-induced trapped charges have been shown not to affect oxide leakage current nor breakdown properties of oxides thicker than 10 nm, [148] but have been observed to increase oxide leakage current and reduce breakdown voltage for ultrathin ($<$ 4 nm in thickness) oxides through electron trap assisted tunneling for total dose irradiations greater than 1 Mrad (Si) [149]–[151]. SNL found no detectable radiation-induced leakage current for 70 nm oxides grown on n-type silicon by rapid thermal processing at 1000 °C in pure oxygen or N_2O, and irradiated by 10 keV X-rays to 20 Mrad (SiO_2). The trapping of radiation-induced electrons in the oxide near the polysilicon interface, however, has been found to modify the reliability related Fowler–Nordheim injection characteristics of the interface [152].

7) Long Term Postradiation Response:

a) $N_{\rm ot}$ annealing: Charge trapped in deep electron and hole traps in oxides has been found to remain trapped for times varying from hours to years, depending on temperature and electric fields. These space charges, which are not in electrical communication with the active silicon regions, however, do have a long term annealing behavior. Tunneling and thermal detrapping mechanisms have been found to be responsible for the long term annealing of trapped holes near the silicon dioxide/silicon interface; the reduction of the charge density is found to have a logarithmic time dependence for both mechanisms. At room temperature tunnel annealing dominates; and at temperatures above 75 °C to 100 °C thermal emission becomes important [153]–[155], [18], [156]–[158]. Shallow electron traps anneal faster than deep traps, and exhibit a response similar to compensated E' centers [159].

Using first principles quantum mechanical calculations, the Air Force Research Laboratory (AFRL) has provided insights regarding the oxide trapped-hole annealing process [160]. These results support the Harry Diamond Laboratory (HDL) model for reverse annealing [161], [162] and provide an electronic structure explanation for the process. Localized holes form a metastable, dipolar complex, without restoring the precursor Si–Si dimer bond upon electron trapping. During an applied negative field, these charge up neutral dipolar complexes that easily can release the weakly bonded electron, exhibiting a reverse annealing condition, where again there exists a positive fixed oxide charge.

The annealing of radiation-induced oxide charge is enhanced by the presence of hydrogen diffused into irradiated oxide at room temperature, while at the same time increasing the density of interface states for MOS structures biased under both positive and negative voltages. The cracking sites for the hydrogen were modeled as not being due to E' centers [163]. In corroboration, it has been found that hydrogen impregnation of synthetic SiO_2 glass suppresses formation of radiation-induced E' centers but enhances formation of oxygen-deficient centers (Si–Si bond) [164]. Thermal annealing studies of irradiated devices have been performed, including those for:

1) aluminum-gate inverters (hard and soft) from -140 °C to 375 °C [165];
2) aluminum-gate inverters, activation energies of thermal annealing [166], [167];
3) aluminum-gate NMOSFETs, reversible positive charge [168];
4) aluminum-gate capacitors (n-type Si), flat-band condition [169];
5) aluminum-gate capacitors, rapid annealing, activation energies [157];
6) silicon-gate NMOSFETs, diffusion of a small molecular species [170];
7) silicon-gate MOSFETs, interface traps [171];
8) silicon-gate NMOSFET/SOS, open and closed geometry [172];
9) silicon-gate MOSFETs/SOS activation energies [173];
10) silicon-gate ($n+$ and $p+$), 4.5 nm oxide, radiation-induced oxide leakage [174];
11) silicon-gate CMOS circuits (various commercial types) [175];
12) silicon-gate commercial power VDMOSFETs [176], [177];
13) PMOS dosimeters [178];
14) commercial power MOSFETs, prediction based on isochronal anneals [179];
15) C^2L 1802 microprocessor, rapid annealing [180];
16) 16 Kb DRAM [181].

b) Threshold Shifts Caused by Switching Oxide Traps: Researchers at SNL discovered, through switched polarity annealing studies, that the radiation-induced net

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

positive charge trapped within the oxide was not removed by the aforementioned annealing processes, but was only charge compensated; thus, only temporarily neutralized [182]. By tunneling electrons from the silicon into the oxide, they annealed an irradiated N-channel MOS transistor (100 °C with +10 volts applied to the gate electrode) for a week until the oxide trapped charge, determined from the mid-gap voltage shift, was annealed out to the preradiation value. Then, they applied a negative 10 V to the gate and continued the annealing at 100 °C. Within one day the initial postradiation value of positive charge was restored. This work was reproduced and verified by NRL and HDL workers [183], [161]. Subsequently, the HDL workers carried out an extensive systematic study and modeling of the negative-bias reverse-annealing mechanism [161], [162], [184]. They observed that charge tunneled in and out of hole traps, reversibly. The magnitude of this effect depends on oxide processing—greater in hardened oxides than in soft oxides. They called this effect "negative bias instability" and modeled the effect as being caused by switching oxide traps, related to E' centers measured by ESR. (See Section VI-C.) The SNL workers labeled these switching oxide traps "border traps" [185], [186] because the traps are located very near the interface. The switching oxide traps, or so-called border traps (or slow states), are not in communication with the silicon as are interface traps ($N_{\rm it}$), nor are they as isolated as oxide traps ($N_{\rm ot}$).

The model for the switching oxide trap put forth by the HDL group is based on the E' center which, before it trapped a hole, was a Si–Si bonded oxygen vacancy, where each silicon is back-bonded to three oxygen atoms. After trapping a hole and breaking the Si–Si bond, one of the Si atoms possesses a single electron in a dangling bond while the other Si atom traps a hole becoming net positive in charge. When this positively charged defect complex captures an electron during annealing (through tunneling or thermal excitation), the electron is trapped on the silicon with the dangling bond which then becomes negative in charge. The other silicon in the complex with the broken Si–Si bond remains positive in charge, thus, creating with the nearby negative charge a dipole structure which, as a complex, is neutral in charge and no longer paramagnetic (and, therefore, not detectable by ESR) [187], [188]. Subsequent work at NRL has shown that the radiation-induced slow states are caused not *only* by E' centers but *also* by hydrogen related centers in the oxide [189].

c) Threshold shifts due to interface state buildup and annealing: Interface states, due to defect-related traps, are electronic levels located spatially at the dielectric/silicon interface and energetically within the band gap of the active silicon [190]. These states are electronically in communication with the silicon. Interface traps outside the silicon band gap are considered as fixed charge and not as interface states, since they do not communicate directly (on the time scale of the measurements) with the silicon [101]. Interface states are amphoteric in nature, i.e., when located in the upper half of the band gap they behave as donors (positive charge state) and when located in the lower half of the band gap they behave as acceptors (negative charge state) [191]. There is charge neutrality at mid-gap only when the densities of both types are equal.

Radiation-induced interface state buildup is a complex process, depending on time scale, oxide thickness, temperature, and electric field (as well as processing). Kinetics include the transport of holes, radiolytic hydrogen (ions and atomic hydrogen), and defects at the oxide/silicon interface (called P_b centers, detected by ESR. (See Section III-C.) However, it has been argued that not all of the radiation-induced interface states $N_{\rm it}$ are related to P_b centers [189]. The HDL researchers have provided a review paper of work through the 1980s, including mechanisms for the prompt and delayed [192] components of $N_{\rm it}$ [193]. Subsequent aspects of time, oxide thickness, and applied field dependencies of $N_{\rm it}$—including the role of hydrogen—have been provided by NRL and SNL [194], [195], [185]. Hydrogen diffused into an irradiated MOS structure at low temperatures (room temperature and 125 °C) enhances the buildup of interface states [163]. Analyses of the kinetics and chemistry of process- and radiation-induced interface trap annealing, including the important role of hydrogen, have been published [196]–[198], [406]. Contradictions between the radiation effects model for interface state formation [192] and hydrogen-annealing models [199] are still being studied [200].

d) Threshold Shifts due to Rebound or Super-Recovery: After both $N_{\rm ot}$ and $N_{\rm it}$ have been generated, $N_{\rm ot}$ continues to anneal out, according to $\ln t$ (where t is time); whereas, the interface states generally do not anneal out with time. After most of the positive charged $N_{\rm ot}$ anneals out, especially at elevated temperatures [201], the negatively charged interface traps (due to acceptor type interface states) remain, causing a positive shift in threshold voltage for N-channel MOS transistors. If this positive shift is great enough and produces a threshold voltage greater than the initial value (super-recovery), device failure, as well as performance degradation, may occur [182]. This condition, called rebound, does not occur for P-channel devices since the interface states for this device are donor type (positive charge), so that the $N_{\rm it}$ charge adds to the positive charge of $N_{\rm ot}$.

8) Acceptor Neutralization: It has been shown that radiolytic atomic hydrogen, released during irradiation, deactivates boron acceptors in the near silicon surface region [202]. The neutralization of boron by atomic hydrogen reaches a maximum at 100 °C [203]. Most shallow acceptor levels due to boron in silicon can be neutralized by atomic hydrogen at temperatures between 65 °C and 300 °C, causing a sixfold increase in resistivity [204]. It has been suggested that the low temperature aspects of hydrogen related acceptor neutralization may be associated with the transitions and reversal aspects of enhanced-low-dose-rate-sensitivity (ELDRS), related to packaging related heat treatments, burn-in, reliability screens, and aging effects [205], [206], [31], [32]. Acceptor neutralization effects due to atomic hydrogen also have been found to occur for other acceptors in silicon, such as aluminum, gallium, and indium, but do not occur for donors (for temperatures between 100 °C and 300 °C) [207]. A technique to separate irradiation-induced charges ($N_{\rm ot}$ and $N_{\rm it}$) in the presence of hydrogen-deactivated dopants has been published [111]. Neutralization of acceptors causes a negative shift in the capacitance–voltage (C–V) curve, just as trapped positive charge does [208]. Furthermore, the neutralization effect has

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

been modeled to include radiolytic proton $(H+)$ drift, as well as atomic hydrogen [209]. Both types of radiolytic hydrogen have been used to demonstrate that irradiation-induced positive oxide charge $(N_{\rm ot})$ can be predominantly trapped protons (not holes) and, thus, be ionic in nature [210].

9) Reliability: The dominant long-term reliability problem with CMOS technology is related to the oxide trapping of hot carriers. Hot carrier reliability has been found to be degraded by TID oxide trapping [211]. However, it was determined by the SNL workers that hot-carrier effects and hardening are not independent phenomena and that modified processing used for radiation hardening, in some cases, can also improve hot carrier reliability [212]. This improvement in hot carrier reliability was verified in radiation-hardened IC production [213].

B. IC Effects

TID radiation effects impact the MOS IC functionality, dc, and ac performance characteristics [214]. Affected dc parameters include quiescent supply current (standby-current), noise margin, and output drive levels. Affected ac parameters include risetime, falltime, and propagation time. These parameter changes can cause a significant degradation in MOS IC performance. Each of the above parameters is affected by factors such as: dose, dose rate, device design, operating temperature, and postradiation anneal time, all of which contribute to the complexities associated with understanding and predicting performance. For instance, because MOS radiation damage effects have a strong bias dependence, nonuniform changes in circuit performance can occur, depending on different bias conditions, cell types (NOR versus NAND), operating conditions (static versus dynamic), sensitivity to leakage current, circuit race margins, and output levels.

The principal causes of radiation-induced circuit failure have been reported as: 1) an inability to switch from one state to another and 2) increases in standby power [215]. Four distinct radiation-induced failure modes are responsible for CMOS IC performance [216]:

1) power-related failure due to leakage current increasing standby power $>$ limit;
2) static failure, where increased N-channel leakage current combined with decreased P-channel drive generates nodes in indeterminate logic states;
3) dynamic failure where delays along a signal path are too large for synchronous operation;
4) dynamic failure where increases in P-channel threshold voltage inhibit switching.

Since the basic causes of degradation and failure are all related to trapped oxide and interfacial charges (as discussed above) it can be understood how the IC damage effects would depend on many operating parameters, such as: irradiation dose, dose-rate, temperature, electrical biases and clocking, as well as postradiation time. As an example, a circuit statically biased 100% of the time during irradiation usually is more radiation sensitive than one cycled, which is usually more sensitive than one that is off 100% of the time during irradiation [215]. It has been shown that selected circuits (irradiated and degraded by exposure to ionizing radiation with electrical bias applied) can be recovered subsequently by exposure to ionizing radiation without applied bias using a phenomenon known as radiation-induced charge neutralization (RICN) [217]. Furthermore, the total dose hardness of SRAMs can vary by more than a factor of three between laboratory irradiation dose rates of 200 rad (Si)/s and a realistic dose rate, such as 0.02 rad (Si)/s, for space applications [218]. Additional details of how radiation affects IC performance and reliability are discussed below.

1) Speed: TID irradiation has been shown to degrade IC speed by increasing propagation delay in logic circuits [219], [220] and access time in memories [218]. Timing delays related to internal logic-gate delays, fanout-induced drive delays, differences in output rise, and fall times for each gate, and the effects of transistor drive and leakage differences caused by TID and transient ionization radiation environments have been simulated using Very High Speed Integrated Circuit Hardware Description Language [221]. Note that increasing propagation delay is related to the threshold voltage shifts of the n- and p-channel transistors. However, as noted above, threshold voltage shifts have all but disappeared as a concern for hardening deep submicron ICs.

2) Functional Failure: Functional failure of CMOS ICs due to TID exposure at dose rates greater than 5 rad (Si)/s usually is preceded by a rapid increase in standby current, [222] due to oxide trapped holes. However, at dose rates typical of space environments (<0.1 rad (Si)/s) failure occurs at a different dose, due to radiation-induced interface traps after the oxide-trapped holes have annealed out of vulnerable regions such as the field oxide [223]. Differences in failure dose due to static versus dynamic biasing during low dose-rate TID irradiation were observed by SNL [224]. The radiation-induced parametric characteristics of memory ICs also are sensitive to the electrical patterns stored in memory during irradiation [214], [225]; and, in some cases, these patterns are burned into the memory after irradiation [226]. The SNL workers have set forth a simple method to determine the radiation and annealing biases that produce the worst case CMOS SRAM postradiation response [227].

V. Parameters Influencing MOS Radiation Effects

A. Material Properties

The particular materials used for gate electrodes, dielectric film regions, and substrates for MOS structures, as well as the associated defects and impurities, impact TID radiation effects and hardening methodologies. A valuable resource for insights into radiation effects for silicon dioxide is the literature regarding radiation effects in bulk glass and optical fibers [228], [229], [100], [230]–[233].

1) Gate Electrode Material: Polysilicon (poly) gate structures are usually more radiation sensitive than aluminum gate devices, probably due to the elevated temperature of processing required for deposition and doping of the polysilicon films [104], [234]. However, HAC was able to develop a silicon gate process that is just as hard as an Al gate process [70]. Some workers have found that p^+ poly gate structures are harder to TID than n^+ poly gate devices [235].

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

Low resistivity metal silicides are used over polysilicon in order to reduce interconnect losses for high-speed performance. However, depending on the choice of metal silicide and the thickness of the underlying polysilicon, dose enhancement may affect the TID response. For example, tungsten over 150 nm of polysilicon produces nearly two times the dose enhancement caused by $TiSi_2$ over the same thickness of polysilicon [236].

Refractory gate materials, such as molybdenum (Mo) and tungsten (W), have been found to provide less radiation-induced shift than aluminum gate structures over the same oxides [237], [238]. Because its work function can be controlled by nitrogen implantation, Mo gate material is now being pursued as a single-metal dual-work function technology to replace p^+ and n^+ polysilicon [239]. Other materials, such as Ag, Sn, In, and Pb (used as MOS gates) cause more radiation-induced trapped charge than Al [240], [19]. These results have been correlated to differences in interfacial strain caused by the different gate materials [240].

2) Dielectric films: Radiation-induced threshold voltage shifts vary for different gate dielectric materials, e.g., silicon nitride over silicon dioxide [241], P_2O_5 over silicon dioxide [45], aluminum oxide [47], as well as for silicon dioxide from different suppliers [242], aluminum implanted silicon dioxide, and chromium doped silicon dioxide [19], [58], [243].

Except for niche applications, like radiation-hardened cryogenic MOS [244] and nonvolatile memory [245] (where dual dielectric films of silicon nitride over silicon dioxide are used), nearly all generations of MOS technology use silicon dioxide gate dielectric films. However, for MOS technology with submicron gate length devices where dual poly gates (p^+ and n^+ doping) are used, silicon nitride/silicon dioxide structures are incorporated. Silicon nitride blocks the diffusion of boron from penetrating into the channel region, preventing unintentional threshold voltage shifts. A 5 nm nitrided oxide has been successfully produced by Honeywell for 0.25 μm radiation hardened CMOS/SOI technology [246].

For dielectric films, other than thermally grown oxides (such as deposited and buried oxide films), shallow [247], as well as deep [248] electron and hole traps need to be considered. As noted previously, the observed trapped charge buildup in these films is the net difference between the trapped positive and negative charges. The electron and hole traps in dielectric films can be measured separately by various techniques, including: avalanche injection [25], [249], [250], photo-injection [251]–[253], and thermally stimulated current (TSC) measurements [254], [120], [255]–[257]. The actual radiation-induced threshold voltage shift due to $N_{\rm ot}$ is basically the difference between the effects of trapping holes and electrons. Processing affects both in complex ways.

Because of continuous scaling, thermal oxides have been thinned to the point (<2 nm) where increasing tunnel currents appear to limit further evolution in technology feature size without changing gate dielectric material. High dielectric constant (high k) materials are now being considered for gate dielectric use. Such as with the higher dielectric constant of aluminum oxide ($k = 9$) compared to that of silicon dioxide ($k = 3.8$), for an equivalent electrical capacitance, aluminum oxide films will be thicker and thus can be more robust [50], [51].

3) Silicon substrate crystal orientation: Early studies of the silicon orientation dependence of TID effects were flawed. First, a study by HAC did not consider the thickness dependence of TID effects. Since the oxide growth rate is greater on $\langle 111\rangle$ than $\langle 100\rangle$ samples (which were oxidized together for the same amount of time), devices with different oxide thickness were compared, 129 versus 103 nm [64]. Using the oxide thickness-cubed (t^3) relationship [65] of threshold voltage shift, it can be seen that the saturated values of radiation-induced threshold shift can be reconciled by these thickness differences. Secondly, a silicon orientation study by RCA [258] used nonstandard processing (RF-heating and helium annealing) that is known to make a difference in oxide trapping [43], [259].

Subsequent to the aforementioned studies, it was found that silicon orientation does make a difference in radiation-induced interface trap transformation [260] and in the energy distribution of interface state annealing [261]. The precursors (for dangling-bond type interfacial defects) responsible for the radiation-induced interfacial trapped charge have been identified by ESR as $P_{\rm bo}$ and P_{b1} for $\langle 100\rangle$ orientation silicon (depending on the back-bonding), and as P_b on $\langle 111\rangle$ silicon [262].

4) Oxide impurities: Cleaning the oxidation furnaces with HCl before gate oxide growth was shown to improve TID hardness; however, HCl and trichloroethane (both cleaning agents)—when present during oxide growth (due to residual chlorine remaining in the oxide)—degrade hardness, especially by enhancing the growth of deleterious radiation-induced interface states [59], [61], [263]. However, if the concentration of trichloroethane in the oxygen during oxide growth is maintained at a low enough level, radiation hardness can be enhanced [264]. The particular impurities removed by the cleaning processes have never been identified and correlated quantitatively to TID damage, even though it is known that HCl cleaning reduces heavy metals and sodium.

Studies of sodium profiles by secondary-ion-mass-spectroscopy (SIMS) and bias-temperature stressing on rad-hard and rad-soft oxides show that (during the surface charging inherent to the SIMS measurement) more sodium drifts to the silicon dioxide/silicon interface for soft oxides than for hard oxides [26], [27]. It was not known at the time of these studies, in the early 1970s, that soft oxides are less dense and thus have larger open structural rings that foster greater sodium transport. Demonstrating further that hole trapping is related to more than just oxygen vacancy point defects [265], [266] and is possibly related to the transport of radiolytic hydrogen [210] which is enhanced by larger ring structure in less dense silicon dioxide films [267].

Nitrogen incorporated during growth into oxides and interfaces degrades TID radiation hardness; whereas, devices with oxides grown in partial pressures of argon, instead of nitrogen, do not realize degradation in TID hardness [24]. Postoxidation anneal (POA) at 1000 °C in nitrogen degrades TID hardness more than POA performed at 1000 °C in an argon ambient [25]. In addition to nitrogen related hole traps [268], the POA heat treatments concomitantly create oxygen vacancy type hole traps [269], it is thought, through the reduction of the oxide caused by the silicon's gettering of oxygen [270]. Of course, the role played by the nitrogen will depend on how and where

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

it is bonded; i.e., in the oxide, back-bonded to oxygen, or at the interface back-bonded to silicon.

Researchers at Yale University found that fluorine doping of gate and field oxides provides improved radiation hardness [271], [272]; whereas, boron doping of gate oxides (10–25 nm in thickness) through the use of p^+ poly gates or by boron implantation of the oxide was found to reduce radiation-induced positive charge trapping [235].

Work at SNL demonstrated that water contamination in dry process tubes (used for oxidation, anneal, and sintering) degraded hardness [61]. However, studies at RCA found that trace water levels—ranging from 16 to 50 000 ppm during nine different runs of dry oxidations at the same temperature as the SNL oxidations—had no influence on hardness [107]. The reasons for these differences were never resolved.

Subsequent work at SNL determined that hydrogen introduced into thermally grown dry oxides during high temperature anneals ($\sim$850 °C) increased the number of radiation-induced trapped oxide charges and prompt (1 ms to 10 s) interface states [273]. However, when the hydrogen content was measured by nuclear reaction analysis (NRA) techniques [274], [275], it was observed that the samples with greater hydrogen content had less radiation-induced oxide charge and interface states [276]. The cited NRA results are for the total amount of hydrogen, which includes hydrogen that is tightly bound in the oxide structure. Perhaps future studies will explore whether the radiation sensitivity can be correlated to the mobile hydrogen content, since it has been shown that H^+ may account for much of the observed radiation-induced N_{ot} [277].

5) Oxide defects: Radiation-induced oxide hole trapping, which usually causes a net positive space charge in the various oxides of MOS devices, is one of the two dominant damage mechanisms of MOS TID radiation effects. (The other damaging mechanism is radiation-induced interface states.) Hole traps have been modeled as being related to defects found in an oxygen deficient oxide-transition layer possessing excess silicon near the Si/SiO_2 interface. This layer is believed to be caused by incomplete oxidation of the silicon [278]–[282]. Excess silicon near the Si/SiO_2 interface is due to oxygen vacancies in the noncrystalline silicon oxide structural network manifested as Si–Si bonds, the precursor of the deep hole trap. The hole trap is formed after the Si–Si bond is broken during the capture of a radiation-induced hole. The defect complex is detectable using ESR as an E' center (the portion of the defect complex containing an unpaired electron) [54], [283], [230]. The other half of the defect complex, a positively charged silicon atom back-bonded to three oxygen atoms in the oxide network, has been considered (for more than 15 years) as *the* irradiation-induced trapped positive charge due to trapped holes [81], [56]. However, some authors believe trapped protons (H^+) also play a role in irradiation-induced positive trapped charge in silicon dioxide [210], [284], [277], [285]. Even though new sensitive diagnostics have recently shown that the thermally grown oxide/silicon interface is very abrupt (less than 1–2 monolayers thick) [286] the existence of oxygen vacancies (as suggested by ESR results) cannot be disproven.

6) Oxide structure: Radiation-induced positive charge trapping was found by NRL to be correlated directly to the mass density (as measured optically by spectroscopic ellipsometry) of thermally grown and buried silicon dioxide films, and the density depends on film growth and annealing conditions [287], [265]. In corroboration, it has been shown recently, using grazing incidence X-ray reflectivity techniques, that thermal annealing in argon (at 1000 °C for 30 min) of silicon dioxide films on silicon, indeed, causes a density decrease due to swelling [288]. This finding agrees with the swelling of annealed oxides observed earlier using spectroscopic ellipsometry [289]. The growth rate of thermal oxides depends on the transport of O_2 through the oxide and is enhanced by structural channels formed during oxide growth [290]. Channels through the oxide, as manifested by enhanced oxide growth rate, are enhanced further by annealing and contribute to reduced density, which correlates to greater radiation sensitivity. Using the permeability of hydrogen as a density probe, NRL found that an increase in density near the oxide/silicon interface suggesting a smaller Si-O ring size near the interface [267]. Positron annihilation spectroscopy also has been used to determine the density profile of the oxide in a nondestructive manner and has confirmed that thermally grown oxide does, indeed, have a density increase near the silicon/silicon dioxide interface [291]. Furthermore, irradiation of silicon dioxide by neutrons, X-rays, gamma rays, electrons, and ions also causes permanent oxide density changes [292], [293].

B. Electric Field

Every MOS hardening effort should consider the details of device and integrated circuit electric field configurations. Fortunately, computer simulation and computer-aided design (CAD) capabilities have made this task less difficult than it was decades ago.

The polarity [294], [62] and magnitude of applied electrical biases (dc and ac) during and after irradiation have a major affect on trapped bulk and interfacial charges because the following TID mechanisms depend on electric field: 1) radiation-induced charge yield; 2) the transport of radiation-induced electrons, holes, and radiolytic hydrogen; and, 3) the capture cross sections for trapping and detrapping of radiation-induced electrons and holes. Therefore, for hardening purposes, design and layout of MOS devices and circuits should include managing and controlling electric fields, especially fringing fields. Fringing fields extending into oxide isolation regions, [137] such as those at the corners of shallow trenches, [89] need to be controlled. Furthermore, drain engineering with LDDs has been found to reduce TID effects associated with fringing electric fields extending into oxide spacers [213], [295].

1) High fields ($>10^6$ *V/cm*)*, as in gate oxide regions:* Oxide hole trapping at electric field strengths (E) greater than 1 MV/cm decreases with increasing E [296]. This decreasing relationship is caused by an $E^{-1/2}$ dependence of hole trapping cross sections [297], [298]. A rate equation for charge buildup which includes carrier drift, geminate recombination, hole/electron trapping, and effects of internal electric fields has been published [299].

Interface trapping dependence on electric field is more complicated: showing an increase with increasing field for alu-

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

minum-gate MOS devices [258] and a decrease with increasing field for polysilicon-gate devices [300].

2) Low fields ($<10^6$ V/cm), due to fringing fields in isolation oxides: For low applied electric fields, space charge effects [208] and reduced charge yields, as well as changes in charge transport and trapping, need to be considered. For instance, HDL found that the radiation-induced interface state buildup takes place primarily through a "prompt" process where the interface states appear immediately after irradiation with little further buildup with time, and the magnitude of the buildup is only weakly dependent upon applied bias [301]. Hole transport times for low electric fields are extended many orders of magnitude over that observed for the high field case associated with gate oxides. In some cases, the transport is so slow that hole trapping occurs in the interior or bulk regions of the oxide [302]. For such a case with the centroid of radiation-induced trapped holes farther from the silicon/silicon dioxide interface, MOS device and IC characteristics are less degraded.

In some cases, as in thick isolation oxides, hole and electron trapping is controlled by internal electric fields (due to oxide space charge) at high radiation doses (>1 Mrad) [303] and low electric fields [304], [305], [11].

VI. MOS Hardening Technology

Radiation hardening of MOS technologies and ICs requires special procedures in design, layout, and/or processing operations. In addition, special testing operations (collectively known as hardness assurance testing) [67] are required to assure that the finished IC device meets the specified criteria for hardness in its intended radiation environment.

A. Design and Layout

Special design and layout considerations frequently are needed for MOS device and circuit hardening. Such concerns extend from the basic device design and layout as far as the details of chip architecture for various macro cells.

Parasitic field oxide (FOX) transistors using unhardened commercial field oxides usually limit hardness to between 10 and 50 krads (possibly to 100 krads for very low TID dose rates) due to field inversion effects. Large increases in quiescent supply current with radiation dose are indicative of field inversion problems. For LOCOS lateral isolation, the region where the thick field oxide thins down to the thin gate oxide (known as the bird's beak region) is high in mechanical stress, causing it to be very radiation sensitive [306], [307]. Fringing fields from the source to drain bias coupled with the polysilicon gate bias cause a high field situation [308], [137]. The electric fields in the lateral isolation region can be controlled for hardening purposes (attaining hardness levels of 50 to 100 Mrad) using an additional polysilicon electrode called a field shield [309], [310]. When a radiation-hardened field oxide is not available, and standard commercial lateral isolation techniques are used, the following procedures have been shown to provide hardness of 100 krad [311].

1) Polysilicon should not extend over the well- to-substrate boundary;
2) And:
   a) adjacent N^+ source/drain regions should not be allowed without an intervening channel stop (P^+),
   b) source/drain implants should be nested inside the thin oxide region,
   c) edgeless (sometimes called re-entrant) N-channel transistors should be used.

Edgeless-transistor and channel-stop approaches essentially tradeoff component density and performance for radiation hardness. Nevertheless, RCA, in the late 1970s, produced radiation hardened (300–500 krad) 6 μm silicon-gate C^2L (*closed COS/MOS*) [312], CMOS processors (CD 1802) [313], 1 Kb and 4 Kb SRAMs, and 8 Kb ROMs using edgeless transistors with a radiation-hardened, silicon dioxide gate-dielectric [49], [314], [315].

The aforementioned hardening approach, using edgeless transistors, coupled with guardbanding, is again being implemented in order to have commercial unhardened semiconductor foundries fabricate radiation-tolerant (100 krad) circuits in advanced (0.25 μm) CMOS technologies [316]. Hardening by design (HBD) can produce radiation tolerant ICs that rival the best commercial devices in terms of speed and power. The drawbacks of HBD become evident when manufacturing very complex high density ICs. Changes required in design and layout compromise device density and, to a lesser degree, device performance. With even more robust design enhancements (with the concomitant performance tradeoffs), HBD can be used to fabricate VLSI circuits hardened to 1 Mrad(Si) [317] and 100 Mrad(Si) using commercial foundries [318]. The single largest challenge (and perhaps cost) is the front-end work to customize the design tools to use commercial semiconductor foundries for radiation hardening.

Additional specific device design and layout procedures for hardening are available:

1) metal gate CMOS [65];
2) silicon-gate bulk CMOS [300], [319]–[321];
3) silicon-gate bulk CMOS hardened cell family [322];
4) silicon-gate CMOS/SOS standard-cell circuits[323];
5) SRAM circuits [324];
6) microprocessor circuits [325];
7) nonvolatile memory[326];
8) power MOSFETs [327], [328];
9) CCDs [329];
10) ASIC technologies [316];
11) CMOS APS (active pixel sensors) [330], [331].

B. Processing

In general, all oxide regions of thickness >10 nm, not hardened by design, need to be processed to minimize the number of hole traps and/or, judiciously, use deep electron traps and recombination centers to produce as little net positive charge as possible. Furthermore, techniques such as ion implantation and layered films controlling the location of trapped charges also are effective in radiation hardening oxide regions. The actual recipes for process hardening, especially for field oxides, usually are proprietary in nature. In addition to the general process-related and geometry considerations

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

for radiation-induced threshold voltage shifts (previously presented in Section IV-A1), it is important to review the relationships of both electron and hole traps to processing details. Radiation-induced charge is trapped at pre-existing oxide and interfacial defects and at defects caused by the transport and trapping of radiation-induced charges and radiolytic hydrogen [332], [266], [98], [258], [62]. After having been transported close to the oxide/silicon interface, a fraction of the holes are trapped in deep hole traps. The trapped holes then create a positive space charge that usually is located within 300 A of the silicon/silicon dioxide interface (with a centroid of 50–100 A from the interface) for thermally grown oxides [279], [333]. For many years, the accepted model for creation of the precursor defects responsible for trapping the irradiation-induced holes has been attributed to oxygen vacancies near the oxide/silicon interface [334]. However, in the 1990s, efforts in Europe and at NRL have attributed a portion of the trapped positive charge to be due to hole trapping at hydrogen related defects (strained silicon-oxygen bonds near the interface that trap both holes and radiolytic hydrogen) [332], [266], [98].

1) Processing Dependencies of Hole Traps: As we discussed above, the radiation response of oxides as a function of processing is complex. Hole trapping (as measured by the flat-band voltage shifts of capacitance-voltage (CV) curves caused by vacuum ultra violet (VUV) optical injection of holes) varies inversely with dry-oxygen growth temperature (without POA) over the range of 900 °C to 1200 °C. POA in argon—at a temperature equal to or greater than the growth temperature—increases hole trapping [335]. However, hole trapping is reduced when thermally grown oxides are annealed in ambients (such as nitrogen or argon) containing sufficient oxygen for the partial pressure of oxygen to exceed the SiO vapor pressure by at least one order of magnitude. In the converse, hole trapping increases for oxides annealed in vacuum [336].

In general, POA in oxygen decreases the number of hole traps in thermal oxides [337]. Hole trapping can be reduced in some thermal oxides by rapid thermal annealing (RTA) in oxygen at 1000 °C, 100 s as the observed optimal time [338]. Attempts to reduce hole trapping in buried oxide material by adding oxygen to reduce the number of oxygen vacancies have not been successful. Using supplemental oxygen implantation or internal oxidation (ITOX) to add oxygen to the buried oxide was found not to reduce hole trapping, [339] but to reduce the capture cross section for electron trapping in the buried oxide [340].

NRL has used optically assisted hole injection techniques to demonstrate that hole trapping in thermally grown silicon dioxide films can be reduced by ion implantation [284]. Workers at the University of Leuven (Belgium) have shown that annealing in pure helium can reduce the hole trap generation during high temperature annealing as compared to annealing in vacuum [341].

In spite of convincing evidence that hydrogen is deleterious to radiation hardness of MOS structures, little effort has been made to derive processes reducing hydrogen content in oxide regions. Looking to the future, where single wafer processing may be practical for low volume fabrication, possibly the cluster tools used for single wafer processing could be designed to reduce and control oxide impurities, such as hydrogen, for radiation hardening purposes. Recent work at NRL demonstrated that hydrogen transport can be reduced by using ion implanted nanoclusters [284].

2) Processing Dependencies of Electron Traps: Electron traps selectively located in appropriate oxide regions can be an important aspect of radiation hardening. The trapping of electrons in energetically deep stable electron traps can be used to charge compensate the radiation-induced positive charge due to trapped holes. For a radiation-hardened 45 nm oxide, SNL found that the density of deeply trapped electrons exceeded the density of electrons in shallow traps by a factor of ~ 3 after radiation exposure, and up to a factor of ten during biased annealing [159].

Shallow electron traps detected in thermally grown oxides can be due to sodium impurities [342] and various water related complexes [343], [344]. Such electron traps can be eliminated by ultraclean technology and high temperature (1000 °C) nitrogen annealing [345] as well as by rapid thermal annealing for 10 s in argon or nitrogen ambients at 600 °C to 800 °C [338]. The density of such electron traps also can be reduced by low temperature (450 °C–500 °C) anneals in forming gas (nitrogen $+10\%$ hydrogen) [346] but not by high temperature (1000 °C) anneals in forming gas (FG) [347]. Furthermore, in cases where these processes are not controlled precisely, the oxide TID effects will vary.

Deep electron traps have been observed (using avalanche-injection techniques) in dry-oxygen grown oxides that did not have a high temperature POA. A POA in nitrogen—at or greater than the growth temperature—has been shown to reduce deep electron traps by $10\times$ [348], [349]. Since nearly all commercial thermally grown oxides have been subjected to a POA in nitrogen at growth temperature during the furnace pull operation (to reduce the initial flat-band voltage), very few deep electron traps will be found. Therefore, in order to radiation harden thermally grown oxides, the nitrogen POA needs to be eliminated or performed at temperatures below the growth temperature to provide the benefit of deep negatively charged electron traps [101]. These techniques of reducing the time/temperature budget of nitrogen POAs were demonstrated by researchers at SNL [24] and were used throughout the 1970s to radiation harden metal-gate CMOS integrated circuits.

Neutral electron traps have been observed in oxides that have been exposed to large doses of ionizing radiation (such as from e-beam and X-ray lithography, plasma-assisted etching and deposition, e-beam metallization, and plasma-assisted oxidation) and then processed through postradiation high temperature annealing. The positive charge from the radiation dose is removed by annealing but the electron trap remains in its neutral state until it traps an electron [350]–[352]. High pressure forming gas (FG) anneals have been shown by IBM workers to remove the neutral electron traps [353].

Performing an unbiased X-ray exposure of MOS transistors, it was found that radiation-induced neutral electron trap densities [354] (a problem for hot-electron reliability) vary inversely with oxidation growth temperature (800 °C to 1000 °C) for both dry-O_2 and dry/wet/dry oxidations [405], [355]. Neutral electron traps also are generated in SiO_2 by the ion implantation of silicon (10^{15} cm^{-2}), [356] as well as oxygen (10^{15} cm^{-2}) [357].

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

Electron traps for radiation hardening purposes can be incorporated into oxides by ion implantation [358], [359], [284]. Electron trapping in buried oxides has been enhanced using silicon implantation [360]. Unlike the defects related to X-ray and electron irradiation, neutral electron traps created by the implantation of silicon (at a dose of 10^{15} cm^{-2}) were not removed by employing the conventional postmetal annealing conditions in FG at 400 °C for times up to 60 min [356].

Large numbers of deep electron traps can be found in deposited oxides, such as those generated by phosphorus in doped oxides [76], carbon contamination in TEOS oxides [90], and silicon nitride [361], [362] films, as well as in buried oxide regions [363], [364], [248], [365]–[368], [247].

3) Hardened Processing: Hardening process details are available for the following devices and structures:

1) metal-gate PMOS [64];
2) metal-gate CMOS [48], [24], [108], [62];
3) deposited oxides [369];
4) field oxides [75], [76], [272], [370];
5) silicon-gate bulk CMOS [73], [300], [371];
6) LOCOS [372], [373], [116];
7) trench isolation [89], [374];
8) nitride-oxide structures [375]–[379];
9) SOS [69], [70], [380]–[382];
10) CCDs [383]–[386];
11) linear CMOS circuits [103], [387];
12) power MOSFETs [388], [389].

C. TID Hardness Prediction by ESR

ESR has been used as a tool to help predict the total ionizing dose hardness for processes under development [390], [1], [391]. ESR can detect point defects in dielectric films by sensing unpaired spins, thus the detection is charge state dependent. ESR spectroscopy has played an important role in the field of MOS radiation effects and hardening in spite of some major correlation difficulties. ESR, coupled with modeling, has helped to determine some of the particular atomic level defects responsible for a portion of the radiation-induced charge in oxide and interfacial regions of MOS devices [392], [393]. It also has been used to predict the influence of particular oxide processing operations on the concentrations of such defects and, thus, on oxide radiation hardness. However, major obstacles were discovered when ESR measurements were applied to fully processed commercial oxides. It was found that in some cases the usual accompanying process-related microcontamination from ion implantation and elsewhere in the production environment could modify the electrical to ESR relationships [390]. Such a situation, where the trapped radiation-induced oxide charge does not track the ESR data, was observed for various oxide implantations [284]. In addition to the macroscopic structural differences of hard and soft oxides detected by optical means, such as by spectroscopic ellipsometry [287], microscopic point defects detected by ESR have been related to total dose radiation hardness. The prevailing model for radiation-induced TID positive charge buildup in oxides is based on the E' point defect as measured by ESR spectroscopy. According to the most widely used model for radiation-induced E' centers, radiation-induced holes (h^+) are trapped at defect centers starting as oxygen vacancy precursors [81]

$$\equiv \text{Si–Si} \equiv +h^+ \longrightarrow \equiv \text{Si}^+ \bullet \text{Si} \equiv \quad (1)$$

where $\equiv$ Si$^+$ • Si $\equiv$ is the E' center, $\equiv$ Si$^+$ is the trapped positive charge (N_{ot}), and $\equiv$ Si indicates that the Si atom is bonded to three O atoms. The precursor of the hole trap (the two weakly bonded Si atoms) results mainly from imperfect oxide growth. This variant of the E' center is called an E'_{gamma} type [394].

Other types of E' centers can result from the interaction of radiation-induced holes (h^+) with SiH groups present in the oxide [395]–[397]

$$\equiv \text{Si-H} + h^+ \longrightarrow \equiv \text{Si} \bullet \ + \text{H}^+. \quad (2)$$

Another possibility for the radiation-induced dissociation of SiH groups results in no E' center (therefore, not observed by ESR) [273]

$$\equiv \text{Si-H} + h^+ \longrightarrow \equiv \text{Si}^+ + \text{H} \quad (3)$$

where $\equiv$ Si indicates that the Si atom is bonded to three O atoms, and $\equiv$ Si$^+$ is the radiation-induced positive charge (N_{ot}). Such hydrogen related processes may contribute to the difficulties in correlating some device and ESR data.

Furthermore, radiation sensitivity related to oxygen-vacancies (defects in MOS devices generated during oxide growth and thought to be responsible for radiation-induced trapped positive charge), as detected by ESR, [80] is enhanced by nearly two orders of magnitude in *bulk* amorphous silica that has been densified by only 3% [293]. However, in the amorphous silica films of MOS devices an equal increase in mass density causes a decrease in radiation-induced positive charge trapping [266].

The lack of a general correlation between radiation-induced trapped charge and ESR also occurs for the SIMOX. Hydrogen anneal processing at 1050 °C increases the E' signal by 10 $\times$ but the trapped positive charge increases only by 10% [398]; the E' signal does not saturate with radiation dose (studied up to 200 Mrad), but the trapped positive charge saturates by 10 Mrad [399], [400]. It has also been shown that in silicon implanted thermally grown oxides the E' center can be related to an electron trap, as well as to a hole trap [401]. In cases where deep electron traps are incorporated to compensate electrically for the deleterious trapped holes, and thus harden the oxide, the associated ESR E' signal is not useful in controlling or optimizing the process. These findings appear to preclude, for now, the general applicability of this technique to fully processed devices; however, for the development of radiation-hardened unit processes, valuable insights can be gained. However, caution needs to be exercised when considering ESR data that has been obtained using corona-charging type "noncontact" methods, since it has been recently shown not to be noninvasive [407].

D. Sources for Hardened MOS Parts

In order to meet requirements for radiation hardened parts not available through commercial suppliers, SNL established a complete design and fabrication capability with a Class-1 (less than 1 particle per ft^3) processing facility to produce hardened

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

custom ICs [325], [402]. This foundry, with its totally separate, isolated equipment bays subsequently served as a beta-site for SEMATECH process-tool qualification efforts and now includes the capability to produce complex radiation hardened CMOS/SOI integrated circuits such as a hardened version of the Intel Pentium processor [403].

Until the mid-1990s, radiation hardened MOS parts could be procured from numerous suppliers who were using design techniques coupled with specialized processing procedures to assure radiation hardness levels greater than 1 Mrad for MOS ICs. Due to dwindling market share for radiation-hardened components, the number of suppliers of strategically hardened parts dropped markedly. For example, as of this writing only one commercial source, Honeywell, remains for hardened CMOS/SOI ICs, and one source, BAE Systems, for bulk CMOS ICs. With the increasing cost of capitalizing, operating and maintaining a state-of-the-art fabrication facility, hardened parts from dedicated wafer fabrication lines cost 10–1000 times that of standard commercial parts. Because of this enormous cost differential, efforts to work with commercial foundries to manufacture radiation-hardened components are being established.

For MOS ICs that need to meet a 100 krad requirement, various specialty electronic design houses are using commercial fabrication foundries for production. For example, Aeroflex UTMC, [317], [404] Peregrine Semiconductor Corporation, Actel and XILINX presently produce qualified hardened (100 krad) parts using commercial foundries. Process modules, design modifications and/or reliance on the intrinsic hardness of the foundry are used to provide total dose hardness. The process modules for hardening can be inserted into the standard commercial process flow [404] and have yielded consistent radiation hardness for more than seven years. This approach may be perceived to be vulnerable to the vicissitudes of foundry availability and the rapid turnover of foundry process updates (that usually affect hardness); however, the experience to date is that no process has been discontinued over the seven years Aeroflex UTMC has been manufacturing components. Commercial standard products are phased in and out rapidly by commercial vendors. A 4 Mb SRAM purchased for a mission today is likely not to be available in six to nine months. One well-documented problem using commercial foundries is that the intrinsic hardness can change dramatically with no apparent cause. For example, at a given foundry the hardness of the 0.25 μ m CMOS technology dropped by a factor of five (going from a hardness of 50–100 krad to 10–20 krad) during a three month period due to commercial fabrication process updates. Of course companies that rely on the "intrinsic hardness" of a commercial foundry are at the greatest risk of unexpected hardening variations. For such situations, a comprehensive hardness assurance program is absolutely necessary and customers should be well informed about the significant risk that radiation hardness could be lost at any time.

ACKNOWLEDGMENT

The authors would like to express their appreciation to L. M. Cohn, R. K. Lawrence, B. J. Mrstik, and A. G. Revesz for helpful suggestions and critique.

REFERENCES

[1] P. M. Lenahan and J. F. Conley, "A physically based predictive model of Si/SiO_2 interface trap generation resulting from the presence of holes in the SiO_2," *Appl. Phys. Lett.*, vol. 71, p. 3126, 1997.
[2] ——, "A comprehensive physically based predictive model for radiation damage in MOS systems," *IEEE Trans. Nucl. Sci.*, vol. 45, p. 2413, 1998.
[3] S. E. Kerns and B. D. Shafer, "The design of radiation-hardened IC's for space: A compendium of approaches," *Proc. IEEE*, vol. 76, p. 1470, 1998.
[4] H.-S. P. Wong, D. J. Frank, P. M. Solomon, C. J. J. Wann, and J. J. Welser, "Nanoscale CMOS," *Proc. IEEE*, vol. 87, pp. 537–570, 1999.
[5] A. H. Johnston, "Radiation effects in advanced microelectronics technologies," *IEEE Trans. Nucl. Sci.*, vol. 45, p. 1339, 1998.
[6] J. R. Srour, "Radiation effects R & D in the 1970s: A retrospective view," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 2660, 1994.
[7] A. H. Johnston and S. B. Roeske, "Total dose effects at low dose rates," *IEEE Trans. Nucl. Sci.*, vol. NS-33, p. 1487, 1986.
[8] J. L. Azarewicz, "Dose rate effects on total dose damage," *IEEE Trans. Nucl. Sci.*, vol. NS-33, p. 1420, 1986.
[9] J. S. Browning, M. P. Connors, C. L. Freshman, and G. A. Finney, "Total dose characterization of a CMOS technology at high dose rates and temperatures," *IEEE Trans. Nucl. Sci.*, vol. 35, p. 1557, 1988.
[10] T. Stanley, D. Neamen, P. Dressendorfer, J. Schwank, P. Winokur, M. Ackermann, K. Jungling, C. Hawkins, and W. Grannemann, "The effect of operating frequency in the radiation induced buildup of trapped holes and interface states in MOS devices," *IEEE Trans. Nucl. Sci.*, vol. NS-32, p. 3982, 1985.
[11] D. M. Fleetwood, L. C. Riewe, J. R. Schwank, S. C. Witczak, and R. D. Schrimpf, "Radiation effects at low electric fields in thermal, SIMOX and bipolar-base oxides," *IEEE Trans. Nucl. Sci.*, vol. 43, p. 2537, 1996.
[12] J. W. Schrankler, R. K. Reich, M. S. Holt, D. H. Ju, J. S. T. Huang, G. D. Kirchner, and H. L. Hughes, "CMOS scaling implications for total dose radiation," *IEEE Trans. Nucl. Sci.*, vol. NS-32, p. 3988, 1985.
[13] M. R. Shaneyfelt, D. M. Fleetwood, P. S. Winokur, J. R. Schwank, and T. L. Meisenheimer, "Effects of device scaling and geometry on MOS radiation hardness assurance," *IEEE Trans. Nucl. Sci.*, vol. 40, p. 1678, 1993.
[14] B. Djezzar, A. Smatti, A. Amrouche, and M. Kechouane, "Channel-length impact on radiation-induced threshold-voltage shift in N-MOSFET's devices at low gamma rays radiation doses," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 1872, 2000.
[15] J. R. Schwank, F. W. Sexton, D. M. Fleetwood, R. V. Jones, R. S. Flores, M. S. Rodgers, and K. L. Hughes, "Temperature effects on the radiation response of MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 35, p. 1432, 1988.
[16] M. R. Shaneyfelt, J. R. Schwank, D. M. Fleetwood, and P. S. Winokur, "Effects of irradiation temperature on MOS radiation response," *IEEE Trans. Nucl. Sci.*, vol. 45, p. 1372, 1998.
[17] M. Simons, "Rapid annealing in irradiated CMOS transistors," *IEEE Trans. Nucl. Sci.*, vol. NS-21, p. 172, 1974.
[18] P. S. Winokur, K. G. Kerris, and L. Harper, "Predicting CMOS inverter response in nuclear and space environments," *IEEE Trans. Nucl. Sci.*, vol. NS-30, p. 4326, 1983.
[19] H. L. Hughes, "A survey of radiation-induced perturbations in metal-insulator-semiconductor structures," in *Proc. IEEE Reliability Physics Symp.*, 1971, IEEE Catalog 71-C-9-Phy 33, p. 1.
[20] A. G. Revesz, "Chemical and structural aspects of the irradiation behavior of SiO_2 films on silicon," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2102, 1977.
[21] A. Revesz, "The role of hydrogen in SiO_2 films on silicon," *J. Electrochem. Soc.*, vol. 126, p. 122, 1979.
[22] D. M. Fleetwood, M. J. Johnson, T. L. Meisenheimer, P. S. Winokur, W. L. Warren, and S. C. Witczak, "$1/f$ noise, hydrogen transport, and latent interface-trap buildup in irradiated MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 44, p. 1810, 1997.
[23] P. E. Bunson, M. D. Ventra, S. T. Pantelides, D. M. Fleetwood, and R. D. Schrimpf, "Hydrogen-related defects in irradiated SiO_2," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 2289, 2000.
[24] G. F. Derbenwick and B. L. Gregory, "Process optimization of radiation-hardened CMOS integrated circuits," *IEEE Trans. Nucl. Sci.*, vol. NS-22, p. 2151, 1975.
[25] J. M. Aitken and D. R. Young, "Avalanche injection of holes into SiO_2," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2128, 1977.
[26] H. L. Hughes, "Dependence of MOS device radiation-sensitivity on oxide impurities," *IEEE Trans. Nucl. Sci.*, vol. NS-19, p. 256, 1972.

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

[27] R. O. Litvinov, V. G. Litovchenko, and C. Radeske, "Effect of surface impurities on radiation-induced changes in MOS structures," *Phys. Stat. Sol (a)*, vol. 22, p. 293, 1974.
[28] R. A. Kohler, R. A. Kushner, and K. H. Lee, "Total dose radiation hardness of MOS devices in hermetic ceramic packages," *IEEE Trans. Nucl. Sci.*, vol. 35, p. 1492, 1988.
[29] S. D. Clark, J. P. Bings, M. K. Williams, D. R. Alexander, M. C. Maher, and R. L. Pease, "Plastic packaging and burn-in effects on ionizing dose response in CMOS microcircuits," *IEEE Trans. Nucl. Sci.*, vol. 42, p. 1607, 1995.
[30] H. J. Barnaby, C. R. Cirba, R. D. Schrimpf, D. M. Fleetwood, R. L. Pease, M. R. Shaneyfelt, T. Turflinger, J. R. Krieg, and M. C. Maher, "Origins of total-dose response variability in linear bipolar microcircuits," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 2342, 2000.
[31] M. R. Shaneyfelt, P. S. Winokur, D. M. Fleetwood, J. R. Schwank, and R. A. Reber, "Effects of reliability screens on MOS charge trapping," *IEEE Trans. Nucl. Sci.*, vol. 43, p. 865, 1996.
[32] M. R. Shaneyfelt, P. S. Winokur, D. M. Fleetwood, G. L. Hash, J. R. Schwank, F. W. Sexton, and R. L. Pease, "Impact of aging on radiation hardness," *IEEE Trans. Nucl. Sci.*, vol. 44, p. 2040, 1997.
[33] M. N. Lovellette, K. S. Wood, D. L. Wood, J. H. Beall, P. P. Shirvani, N. Oh, and E. J. McCluskey, "Strategies for fault-tolerant, space-based computing: Lessons learned from the ARGOS testbed," in *IEEE Aerospace Conf. Proc.*, 2002.
[34] H. L. Hughes and R. R. Giroux, "Space radiation affects MOSFET's," *Electronics*, vol. 37, p. 58, 1964.
[35] S. R. Hofstein and F. P. Heiman, "The silicon insulated-gate field-effect transistor," *Proc. IEEE*, p. 1190, 1963.
[36] H. L. Hughes, "Surface effects of space radiation on silicon devices," *IEEE Trans. Nucl. Sci.*, vol. NS-12, p. 53, 1965.
[37] P. J. Estrup, "Surface effects of gaseous ions and electrons on semiconductor devices," *IEEE Trans. Nucl. Sci.*, vol. NS-12, p. 431, 1965.
[38] J. Raymond, E. Steele, and W. Chang, "Radiation effects in metal-oxide-semiconductor transistors," *IEEE Trans. Nucl. Sci.*, vol. NS-12, p. 457, 1965.
[39] D. C. Sullivan, "Transient radiation-induced response of MOS field effect transistors," *IEEE Trans. Nucl. Sci.*, vol. NS-12, p. 31, 1965.
[40] G. C. Messenger, E. J. Steele, and M. Neustadt, "Displacement damage in MOS transistors," *IEEE Trans. Nucl. Sci.*, vol. NS-12, p. 78, 1965.
[41] D. P. Snowden and T. M. Flanagan, "Transient response of MOS capacitors to high-energy electron irradiation," *IEEE Trans. Nucl. Sci.*, vol. NS-22, p. 2516, 1975.
[42] A. G. Stanley, "Effects of electron irradiation on metal-oxide semiconductor transistors," *Proc. IEEE*, vol. 53, p. 627, 1965.
[43] A. G. Revesz and B. Goldstein, "Electron paramagnetic resonance investigation of the Si–SiO_2 interface," *Surface Sci.*, vol. 14, p. 361, 1969.
[44] C. W. Perkins, "Radiation effects in metal-insulator-semiconductor capacitors as determined from conductance measurements," *Appl. Phys. Lett.*, vol. 12, p. 153, 1968.
[45] C. W. Perkins, K. G. Aubuchon, and H. G. Dill, "Radiation effects in modified oxide insulators in MOS structures," *IEEE Trans. Nucl. Sci.*, vol. NS-15, p. 176, 1968.
[46] R. A. Kjar, J. L. Peel, and C. Y. Wrigley, "Effects of metallic doping on ionization damage in MOSFETS," *IEEE Trans. Nucl. Sci.*, vol. NS-16, p. 207, 1969.
[47] K. H. Zaininger and A. S. Waxman, "Radiation resistance of Al_2O_3 MOS devices," *IEEE Trans. Electron. Devices*, vol. ED-16, p. 333, 1969.
[48] K. M. Schlesier and P. E. Norris, "CMOS hardening techniques," *IEEE Trans. Nucl. Sci.*, vol. NS-19, p. 275, 1972.
[49] H. Borkan, "Radiation hardening of CMOS technologies—An overview," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2043, 1977.
[50] T. Amazawa, T. Ono, M. Shimada, S. Matsuo, and H. Oikawa, "Ultrathin oxide films deposited using electron cyclotron resonance sputter," *J. Vac. Sci. Technol. B*, vol. 17, p. 2222, 1999.
[51] A. Stesmans and V. V. Afanas'ev, "Si dangling-bond-type defects at the interface of (100)Si with ultrathin layers of SiO_x, Al_2O_3, and ZrO_2," *Appl. Phys. Lett.*, vol. 80, p. 1957, 2002.
[52] R. J. Kriegler, "Neutralization of Na^+ ions in HCl-grown SiO_2," *Appl. Phys. Lett.*, vol. 20, p. 449, 1972.
[53] C. L. Marquardt and G. H. Sigel, "Radiation-Induced defect centers in thermally grown oxide films," *IEEE Trans. Nucl. Sci.*, vol. NS-22, p. 2234, 1975.
[54] R. A. Weeks, "Paragmagnetic resonance of lattice defects in irradiated quartz," *J. Appl. Phys.*, vol. 27, p. 1376, 1956.
[55] R. H. Silsbee, "Electron spin resonance in neutron-irradiated quartz," *J. Appl. Phys.*, vol. 32, p. 1459, 1961.
[56] F. J. Feigl, W. B. Fowler, and K. L. Yip, "Oxygen vacancy model for the E_1' center in SiO_2," *Solid State Commun.*, vol. 14, p. 225, 1974.
[57] F. B. Micheletti and F. Kolondra, "Relaxation phenomena associated with radiation-induced trapped charge in Al_2O_3 MOS devices," *IEEE Trans. Nucl. Sci.*, vol. NS-18, p. 131, 1971.
[58] E. E. King, G. P. Nelson, and H. L. Hughes, "The effects of ionizing radiation on various CMOS integrated circuit structures," *IEEE Trans. Nucl. Sci.*, vol. NS-19, p. 264, 1972.
[59] K. G. Aubuchon, E. Harari, D. H. Leong, and C. P. Chang, "Effects of HCl gettering, Cr doping and Al^+ implantation on hardened SiO_2," *IEEE Trans. Nucl. Sci.*, vol. NS-21, p. 167, 1974.
[60] J. L. Peel and G. Kinoshita, "Radiation-Hardened complementary MOS using SiO_2 gate insulators," *IEEE Trans. Nucl. Sci.*, vol. NS-19, p. 271, 1972.
[61] B. L. Gregory, "Process controls for radiation-hardened aluminum gate bulk silicon CMOS," *IEEE Trans. Nucl. Sci.*, vol. NS-22, p. 2295, 1975.
[62] W. R. Dawes, G. F. Derbenwick, and B. L. Gregory, "Process technology for radiation-hardened CMOS integrated circuits," *IEEE J. Solid-State Circuits*, vol. SC-11, p. 459, 1976.
[63] A. London, D. A. Matteucci, and R. C. Wang, "Establishment of a radiation hardened CMOS manufacturing process," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2056, 1977.
[64] K. G. Aubuchon, "Radiation hardening of P-MOS devices by optimization of the thermal SiO_2 gate insulator," *IEEE Trans. Nucl. Sci.*, vol. NS-18, p. 117, 1971.
[65] J. G. Fossum, G. F. Derbenwick, and B. L. Gregory, "Design optimization of radiation-hardened CMOS integrated circuits," *IEEE Trans. Nucl. Sci.*, vol. NS-22, p. 2208, 1975.
[66] J. R. Adams and F. N. Coppage, "Field oxide inversion effects in irradiated CMOS devices," *IEEE Trans. Nucl. Sci.*, vol. NS-23, p. 1604, 1976.
[67] T. J. Sanders, "CMOS hardness assurance through process controls and optimized design procedures," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2051, 1977.
[68] J. L. Peel, R. K. Pancholy, G. J. Kuhlmann, T. J. Oki, and R. A. Williams, "Investigation of radiation effects and hardening procedures for CMOS/SOS," *IEEE Trans. Nucl. Sci.*, vol. NS-22, p. 2185, 1975.
[69] K. G. Aubuchon and E. Harari, "Radiation hardened CMOS/SOS," *IEEE Trans. Nucl. Sci.*, vol. NS-22, p. 2181, 1975.
[70] K. G. Aubuchon, H. T. Peterson, and D. P. Shumake, "Radiation-Hardened CMOS/SOS LSI circuits," *IEEE Trans. Nucl. Sci.*, vol. NS-26, p. 1613, 1976.
[71] J. R. Srour, S. Othmer, and S. C. Chen, "Leakage current phenomena in irradiated SOS devices," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2119, 1977.
[72] J. R. Adams, W. R. Dawes, and T. J. Sanders, "A radiation hardened field oxide," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2099, 1977.
[73] T. J. Sanders, "Silicon gate CMOS on bulk silicon for ionizing radiation environments," *IEEE Trans. Nucl. Sci.*, vol. NS-26, p. 5056, 1979.
[74] T. R. Oldham, A. J. Lelis, H. E. Boesch, J. M. Benedetto, F. B. McLean, and J. M. McGarrity, "Post-Irradiation effects in field-oxide isolation structures," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1184, 1987.
[75] K. Watanabe, M. Kato, T. Okabe, and M. Nagata, "Radiation hardened silicon devices using a novel thick oxide," *IEEE Trans. Nucl. Sci.*, vol. NS-32, p. 3971, 1985.
[76] ——, "Radiation effects of double layer dielectric films," *IEEE Trans. Nucl. Sci.*, vol. NS-33, p. 1216, 1986.
[77] W. L. Warren, P. M. Lenahan, B. Robinson, and J. H. Stathis, "Neutral E' centers in microwave downstream plasma-enhanced chemical-vapor-deposited silicon dioxide," *Appl. Phys. Lett.*, vol. 53, p. 482, 1988.
[78] P. M. Lenahan and P. B. Dressendorfer, "Microstructural variations in radiation hard and soft oxides observed through electron spin resonance," *IEEE Trans. Nucl. Sci.*, vol. NS-30, p. 4602, 1983.
[79] R. A. B. Devine, "Comparative radiation sensitivity study of bulk wet and dry amorphous SiO_2," *J. Non-Cryst. Solids*, vol. 107, p. 41, 1988.
[80] P. M. Lenahan and P. V. Dressendorfer, "Radiation-induced paramagnetic defects in MOS structures," *IEEE Trans. Nucl. Sci.*, vol. NS-29, p. 1459, 1982.
[81] ——, "Hole traps and trivalent silicon centers in metal/oxide/silicon devices," *J. Appl. Phys.*, vol. 55, p. 3495, 1984.
[82] P. M. Lenahan, K. L. Brower, P. V. Dressendorfer, and W. C. Johnson, "Radiation-Induced trivalent silicon defect buildup at the Si–SiO_2 interface in MOS structures," *IEEE Trans. Nucl. Sci.*, vol. NS-28, p. 4105, 1981.
[83] P. M. Lenahan and P. V. Dressendorfer, "An electron spin resonance study of radiation-induced electrically active paramagnetic centers at the Si/SiO_2 interface," *J. Appl. Phys.*, vol. 54, p. 1457, 1983.

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

[84] ——, "Effect of bias on radiation-induced paramagnetic defects at the silicon–silicon dioxide interface," *Appl. Phys. Lett.*, vol. 41, p. 542, 1982.

[85] Y. Y. Kim and P. M. Lenahan, "Electron-spin-resonance study of radiation-induced paramagnetic defects in oxides grown on (100) silicon substrates," *J. Appl. Phys.*, vol. 64, p. 3551, 1988.

[86] L. J. Palkuti and J. J. LePage, "X-ray wafer probe for total dose testing," *IEEE Trans. Nucl. Sci.*, vol. NS-29, p. 1832, 1982.

[87] J. M. Benedetto, H. E. Boesch, F. B. McLean, and J. P. Mize, "Hole removal in thin-gate MOSFET's by tunneling," *IEEE Trans. Nucl. Sci.*, vol. NS-32, p. 3916, 1985.

[88] J. W. Lutze and J. P. Krusius, "Electrical limitations of advanced LOCOS isolation for deep submicrometer CMOS," *IEEE Trans. Electron. Devices*, vol. 38, 1991.

[89] M. R. Shaneyfelt, P. E. Dodd, B. L. Draper, and R. S. Flores, "Challenges in hardening technologies using shallow-trench isolation," *IEEE Trans. Nucl. Sci.*, vol. 45, p. 2584, 1998.

[90] P. M. Lenahan, C. A. Billman, R. Fuller, H. Evans, W. H. Speece, D. DeCrosta, and R. Lowry, "A study of charge trapping in PECVD PTEOS films," *IEEE Trans. Nucl. Sci.*, vol. 44, p. 1834, 1997.

[91] D. B. Kerwin and J. M. Benedetto, "Total dose and single event effects testing of UTMC commercial RADHARDTM gate arrays," in *Proc. IEEE Radiation Effects Data Workshop*, 1998, IEEE Catalog #98TH8385, p. 80.

[92] K. R. Davis, R. D. Schrimpf, F. E. Cellier, K. F. Galloway, D. I. Burton, and C. F. Wheatley, "The effects of ionizing radiation on power-MOSFET termination structures," *IEEE Trans. Nucl. Sci.*, vol. 36, p. 2104, 1989.

[93] D. N. Nguyen, S. M. Guertin, G. M. Swift, and A. H. Johnston, "Radiation effects on advanced flash memories," *IEEE Trans. Nucl. Sci.*, vol. 46, p. 1744, 1999.

[94] R. Katz, G. Swift, and D. Shaw, "Total dose responses of ACTEL 1020B and 1280A field programmable gate arrays," in *RADECS95 Proc.*, 1995, IEEE Doc. 95TH8147, p. 412.

[95] A. Y. Kang, P. M. Lenahan, and J. J. F. Conely, "The radiation response of the high dielectric constant hafnium oxide/silicon system," *IEEE Trans. Nucl. Sci.*, vol. 49, p. 1249, 2002.

[96] K. Neumeier, P. Seegebrecht, and H. P. Bruemmer, "Radiation tolerance of double layer field oxides," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 391, 1992.

[97] R. Fuller, H. Evans, C. Gamlen, B. Czagas, M. Morrison, D. Decrosta, and R. Lowry, "The effect of deposition conditions on the radiation tolerance of BPSG films," *IEEE Trans. Nucl. Sci.*, vol. 43, p. 2565, 1996.

[98] V. V. Afanas'ev and A. Stesmans, "Charge state of paramagnetic E' centre in thermal SiO_2 layers on silicon," *J. Phys.: Condens. Matter*, vol. 12, p. 2285, 2000.

[99] K. L. Brower, P. M. Lenahan, and P. V. Dressendorfer, "Defects and impurities in thermal oxides on silicon," *Appl. Phys. Lett.*, vol. 41, p. 251, 1982.

[100] D. L. Griscom, M. Stapelbroek, and E. J. Friebele, "ESR studies of damage processes in X-irradiated high purity a-SiO_2:OH and characterization of the formyl radical defect," *J. Chem. Phys.*, vol. 78, p. 1638, 1983.

[101] Z. Shanfield, G. A. Brown, A. G. Revesz, and H. L. Hughes, "A new MOS radiation-induced charge: Negative fixed interface charge," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 303, 1992.

[102] S. J. Mathew, G. Niu, S. D. Clark, J. D. Cressler, M. J. Palmer, and W. B. Dubbelday, "Radiation-Induced back-channel leakage in SiGe CMOS on silicon-on-sapphire (SOS) technology," *IEEE Trans. Nucl. Sci.*, vol. 46, p. 1848, 1999.

[103] T. J. Sanders and K. A. Ports, "Radiation-hardened CMOS devices for linear circuit applications," *IEEE Trans. Nucl. Sci.*, vol. NS-25, p. 1465, 1978.

[104] T. V. Nordstrom and C. F. Gibbon, "The effect of gate oxide thickness on the radiation hardness of silicon-gate CMOS," *IEEE Trans. Nucl. Sci.*, vol. NS-28, p. 4349, 1978.

[105] K. Naruke, M. Yoshida, K. Maeguchi, and H. Tango, "Radiation-induced interface states of poly-Si gate MOS capacitors using low temperature gate oxidation," *IEEE Trans. Nucl. Sci.*, vol. NS-30, p. 4054, 1983.

[106] G. W. Hughes, R. J. Powell, and M. H. Woods, "Oxide thickness dependence of high-energy-electron-, VUV-, and corona-induced charge in MOS capacitors," *Appl. Phys. Lett.*, vol. 29, p. 377, 1976.

[107] G. W. Hughes and R. J. Powell, "MOS hardness characterization and its dependence upon some process and measurement variables," *IEEE Trans. Nucl. Sci.*, vol. NS-23, p. 1569, 1976.

[108] K. M. Schlesier and C. W. Benyon, "Processing effects on steam oxide hardness," *IEEE Trans. Nucl. Sci.*, vol. NS-23, p. 1599, 1976.

[109] P. J. McWhorter and P. S. Winokur, "Simple technique for separating the effects of interface traps and trapped-oxide charge in metal-oxide-semiconductor transistors," *Appl. Phys. Lett.*, vol. 48, p. 133, 1986.

[110] A. Torres, O. Flament, C. Marcandella, O. Musseau, and J. L. Leray, "Spatial and spectral oxide trap distributions in power MOSFET's," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 587, 2000.

[111] S. C. Witczak, P. S. Winokur, R. C. Lacoe, and D. C. Mayer, "Charge separation technique for metal-oxide-silicon capacitors in the presence of hydrogen deactivated dopants," *J. Appl. Phys.*, vol. 87, p. 8206, 2000.

[112] D. M. Fleetwood, M. R. Shaneyfelt, J. R. Schwank, P. S. Winokur, and F. W. Sexton, "Theory and application of dual-transistor charge separation analysis," *IEEE Trans. Nucl. Sci.*, vol. 36, p. 1816, 1989.

[113] N. S. Saks and M. G. Ancona, "Generation of interface states by ionizing radiation at 80 K measured by charge pumping and subthreshold slope techniques," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1348, 1987.

[114] R. E. Paulsen and M. H. White, "Theory and application of charge pumping for the characterization of Si–SiO_2 interface and near-interface oxide traps," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 1213, 1994.

[115] S. C. Witczak, K. F. Galloway, R. D. Schrimpf, J. L. Titus, J. R. Brews, and B. Prevost, "The determination of Si–SiO_2 interface trap density in irradiated four-terminal VDMOSFETS using charge pumping," *IEEE Trans. Nucl. Sci.*, vol. 43, p. 2558, 1996.

[116] O. Flament, J. L. Autran, P. Paillet, P. Roche, O. Faynot, and R. Truche, "Charge pumping analysis of radiation effects in LOCOS parasitic transistors," *IEEE Trans. Nucl. Sci.*, vol. 44, p. 1930, 1997.

[117] K. F. Galloway, M. Gaitan, and T. J. Russell, "A simple model for separating interface and oxide charge effects in MOS device characteristics," *IEEE Trans. Nucl. Sci.*, vol. NS-31, p. 1497, 1984.

[118] K. F. Galloway, C. L. Wilson, and L. C. Witte, "Charge-sheet model fitting to extract radiation-induced oxide and interface charge," *IEEE Trans. Nucl. Sci.*, vol. NS-32, p. 4461, 1985.

[119] N. S. Saks, M. G. Ancona, and R. W. Rendell, "Using the hall effect to measure interface trap densities in silicon carbide and silicon metal-oxide-semiconductor devices," *Appl. Phys. Lett.*, vol. 80, p. 3219, 2002.

[120] Z. Shanfield and M. M. Moriwaki, "Critical evaluation of the midgap-voltage-shift method for determining oxide trapped charge in irradiated MOS devices," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1159, 1987.

[121] D. M. Fleetwood, "Long-term annealing study of midgap interface-trap charge neutrality," *Appl. Phys. Lett.*, vol. 60, p. 2883, 1992.

[122] K. G. Druijf, J. M. M. d. Mijs, E. v. d. Drift, E. H. A. Granneman, and P. Balk, "Nature of defects in the Si–SiO_2 system generated by vacuum-ultraviolet irradiation," *Appl. Phys. Lett.*, vol. 65, p. 347, 1994.

[123] H. E. Boesch, F. B. McLean, J. M. Benedetto, J. M. McGarrity, and W. E. Bailey, "Saturation of threshold voltage shift in MOSFET's at high total dose," *IEEE Trans. Nucl. Sci.*, vol. NS-33, p. 1191, 1986.

[124] H. L. Hughes and E. E. King, "The influence of silicon surface defects on MOS radiation-sensitivity," *IEEE Trans. Nucl. Sci.*, vol. NS-23, p. 1573, 1976.

[125] R. K. Freitag, E. A. Burke, C. M. Dozier, and D. B. Brown, "The development of nonuniform deposition of holes in gate oxides," *IEEE Trans. Nucl. Sci.*, vol. 35, p. 1201, 1988.

[126] A. Balasinski and T.-P. Ma, "Impact of radiation-induced nonuniform damage near MOSFET junctions," *IEEE Trans. Nucl. Sci.*, vol. 40, p. 1286, 1993.

[127] A. G. Stanley, "Effect of electron irradiation on carrier mobilities in inversion layers of insulated gate field effect transistors," *IEEE Trans. Nucl. Sci.*, vol. NS-14, p. 266, 1967.

[128] B. A. Girii, A. V. Kondrachuk, S. I. Kornyushin, R. O. Litvinov, and V. I. Shakhovtsov, "The effect of irradiation on the carrier mobility in inversion layers of MOS structures," *Phys. Stat. Sol. (a)*, vol. 22, p. 357, 1974.

[129] J. E. Whitefield, H. D. Southward, and R. J. Maier, "Total dose effects on surface state density, carrier concentration and mobility in MOS layers," *IEEE Trans. Nucl. Sci.*, vol. NS-23, p. 1549, 1976.

[130] F. B. McLean and H. E. Boesch, "Time-dependent degradation of MOSFET channel mobility following pulsed irradiation," *IEEE Trans. Nucl. Sci.*, vol. 36, p. 1772, 1989.

[131] J. H. Scofield, M. Trawick, P. Klimecky, and D. M. Fleetwood, "Correlation between preirradiation channel mobility and radiation-induced interface-trap charge in metal-oixde-semiconductor transistors," *Appl. Phys. Lett.*, vol. 58, p. 2782, 1991.

[132] D. Zupac, K. F. Galloway, P. Khosropour, S. R. Anderson, R. D. Schrimpf, and P. Calvel, "Separation of effects of oxide-trapped charge and interface-trapped charge on mobility in irradiated power MOSFET's," *IEEE Trans. Nucl. Sci.*, vol. 40, p. 1307, 1993.

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

[133] R. L. Pease, S. D. Clark, P. L. Cole, J. F. Krieg, and J. C. Pickel, "Total dose response of transconductance in MOSFET's at low temperature," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 549, 1994.
[134] A. Acovic, C. C.-H. Hsu, L.-C. Hsia, A. Balasinski, and T.-P. Ma, "Effects of X-ray irradiation on GIDL in MOSFET's," *IEEE Electron. Device Lett.*, vol. 13, p. 189, 1992.
[135] K. T. San and T.-P. Ma, "Determination of trapped oxide charge in flash EPROM's and MOSFET's with thin oxides," *IEEE Electron. Device Lett.*, vol. 13, p. 439, 1992.
[136] A. Balasinski and T.-P. Ma, "Ionizing radiation damage near CMOS transistor channel edges," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 1998, 1992.
[137] V. S. Pershenkov, M. S. Chirokov, P. T. Bretchko, P. O. Fastenko, V. K. Baev, and V. V. Belyakov, "The effect of junction fringing field on radiation-induced leakage current in oxide isolation structures and nonuniform damage near the channel edges in MOSFET's," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 1895, 1994.
[138] S. L. Kosier, R. D. Schrimpf, F. E. Cellier, and K. F. Galloway, "The effects of ionizing radiation on the breakdown voltage of P-channel power MOSFET's," *IEEE Trans. Nucl. Sci.*, vol. 37, p. 2076, 1990.
[139] J. A. Babcock, J. L. Titus, R. D. Schrimpf, and K. F. Galloway, "Effects of ionizing radiation on the noise properties of DMOS power transistors," *IEEE Trans. Nucl. Sci.*, vol. 38, p. 1304, 1991.
[140] P. Augier, J. L. Todsen, D. Zupac, R. D. Schrimpf, K. F. Galloway, and J. A. Babcock, "Comparison of $1/f$ noise in irradiated power MOSFET's measured in the linear and saturation regions," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 2012, 1992.
[141] M. D. Ploor, R. D. Schrimpf, and K. F. Galloway, "Investigation of possible sources of $1/f$ noise in irradiated n-channel power MOSFET's," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 1902, 1994.
[142] J. H. Scofield, T. P. Doerr, and D. M. Fleetwood, "Correlation between preirradiation $1/f$ noise and postirradiation oxide-trapped charge in MOS transistors," *IEEE Trans. Nucl. Sci.*, vol. 36, p. 1946, 1989.
[143] T. L. Meisenheimer and D. M. Fleetwood, "Effect of radiation-induced charge on $1/f$ noise in MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 37, p. 1696, 1990.
[144] T. L. Meisenheimer, D. M. Fleetwood, M. R. Shaneyfelt, and L. C. Riewe, "$1/f$ noise in N- and P-channel MOS devices through irradiation and annealing," *IEEE Trans. Nucl. Sci.*, vol. 38, p. 1297, 1991.
[145] D. M. Fleetwood, T. L. Meisenheimer, and J. H. Scofield, "$1/f$ noise and radiation effects in MOS devices," *IEEE Trans. Electron. Devices*, vol. 41, p. 1953, 1994.
[146] V. Berland, A. Touboul, and P. Crevel, "Comparison of the low frequency noise evolution with the oxide trapped charge in irradiated N-MOS transistors," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 561, 1994.
[147] M.-H. Tsai and T.-P. Ma, "Effect of radiation-induced interface traps on $1/f$ noise in MOSFET's," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 2178, 1992.
[148] A. Paccagnella, A. Candelori, A. Milani, E. Formigoni, G. Ghidini, F. Pellizzer, D. Drera, P. G. Fuochi, and M. Lavale, "Breakdown properties of irradiated MOS capacitors," *IEEE Trans. Nucl. Sci.*, vol. 43, p. 2609, 1996.
[149] A. Scarpa, A. Paccagnella, F. Montera, G. Ghibaudo, G. Pananakakis, G. Bhidini, and P. G. Fuochi, "Ionizing radiation induced leakage current on ultra-thin gate oxides," *IEEE Trans. Nucl. Sci.*, vol. 44, p. 1818, 1997.
[150] L. Larcher, A. Paccagnella, M. Ceschia, and G. Ghidini, "A model of radiation induced leakage current (RILC) in ultra-thin gate oxides," *IEEE Trans. Nucl. Sci.*, vol. 46, p. 1553, 1999.
[151] P. Riess, M. Ceschi, A. Paccagnella, G. Ghibaudo, and G. Pananakakis, "Comparison of the electrical and thermal stability of stress- or radiation-induced leakage current in thin oxides," *Appl. Phys. Lett.*, vol. 76, p. 1158, 2000.
[152] A. Scarpa, A. Paccagnella, F. Montera, A. Candelori, G. Ghibaudo, G. Pananakakis, G. Ghidini, and P. G. Fuochi, "Modifications of Fowler-Nordheim injection characteristics in gamma irradiated MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 45, p. 1390, 1998.
[153] T. R. Oldham, A. J. Lelis, and F. B. McLean, "Spatial dependence of trapped holes determined from tunneling analysis and measured annealing," *IEEE Trans. Nucl. Sci.*, vol. NS-33, p. 1203, 1986.
[154] G. F. Derbenwick and H. H. Sander, "CMOS hardness prediction for low-dose-rate environments," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2244, 1977.
[155] P. S. Winokur, "Limitations in the use of linear system theory for the prediction of hardened-MOS device response in space satellite environments," *IEEE Trans. Nucl. Sci.*, vol. NS-29, p. 2102, 1982.
[156] M. Simons and H. L. Hughes, "Short-term charge annealing in electron-irradiated silicon dioxide," *IEEE Trans. Nucl. Sci.*, vol. NS-18, p. 106, 1971.
[157] ——, "Determning the energy distribution of pulse-radiation-induced charge in MOS structures from rapid annealing measurements," *IEEE Trans. Nucl. Sci.*, vol. NS-19, p. 282, 1972.
[158] P. J. McWhorter, S. L. Miller, and W. M. Miller, "Modeling the anneal of radiation-induced trapped holes in a varying thermal environment," *IEEE Trans. Nucl. Sci.*, vol. 37, p. 1682, 1990.
[159] D. M. Fleetwood, P. S. Winokur, O. Flament, and J. L. Leray, "Stability of trapped electrons in SiO_2," *Appl. Phys. Lett.*, vol. 74, p. 2969, 1999.
[160] S. P. Karna, A. C. Pineda, R. D. Pugh, W. M. Shedd, and T. R. Oldham, "Electronic structure theory and mechanisms of the oxide trapped hole annealing process," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 2316, 2000.
[161] A. J. Lelis, H. E. Boesch, T. R. Oldham, and F. B. McLean, "Reversibility of trapped hole annealing," *IEEE Trans. Nucl. Sci.*, vol. 35, p. 1186, 1988.
[162] A. J. Lelis, T. R. Oldham, H. E. Boesch, and F. B. McLean, "The nature of the trapped hole annealing process," *IEEE Trans. Nucl. Sci.*, vol. 36, p. 1808, 1989.
[163] B. J. Mrstik, "Post-Irradiation formation of Si–SiO_2 interface states in a hydrogen atmosphere at room temperature," *J. Elect. Mat.*, vol. 20, p. 627, 1991.
[164] Y. Ikuta, K. Kajihara, M. Hirano, S. Kikugawa, and H. Hosono, "Effects of H_2 impregnation on excimer-laser-induced oxygen-deficient center formation in synthetic SiO_2 glass," *Appl. Phys. Lett.*, vol. 80, p. 3916, 2002.
[165] V. Danchenko, P. H. Fang, and S. S. Brashears, "Thermal annealing of radiation damage in CMOS ICS in the temperature range $-140^{\circ}C$ to $+375^{\circ}C$," *IEEE Trans. Nucl. Sci.*, vol. NS-29, p. 1716, 1982.
[166] V. Danchenko, E. G. Stassinopoulos, P. H. Fang, and S. S. Brashears, "Activation energies of thermal annealing of radiation-induced damage in n- and p-channels of CMOS integrated circuits, Part I," *IEEE Trans. Nucl. Sci.*, vol. NS-27, p. 1658, 1980.
[167] V. Danchenko, P. H. Fand, and S. S. Brashears, "Activation energies of thermal annealing of radiation-induced damage in n- and p-channels of CMOS integrated circuits, Part II," *IEEE Trans. Nucl. Sci.*, vol. NS-28, p. 4407, 1981.
[168] V. V. Emelianov, G. I. Zebrev, V. N. Ulimov, R. G. Useinov, V. V. Belyakov, and V. S. Pershenkov, "Reversible positive charge annealing in MOS transistor during variety of electrical and thermal stresses," *IEEE Trans. Nucl. Sci.*, vol. 43, p. 805, 1996.
[169] J.-G. Hwu, G.-S. Lee, S.-C. Lee, and W.-S. Wang, "Residual charge effect on the annealing behavior of Co-60 irradiated MOS capacitors," *IEEE Trans. Nucl. Sci.*, vol. 35, p. 960, 1988.
[170] D. B. Brown, D. I. Ma, C. M. Dozier, and M. C. Peckerar, "Thermal annealing of radiation induced defects: A diffusion-limited process?," *IEEE Trans. Nucl. Sci.*, vol. NS-30, p. 4059, 1983.
[171] A. J. Lelis, T. R. Oldham, and W. M. DeLancey, "Response of interface traps during high-temperature anneals," *IEEE Trans. Nucl. Sci.*, vol. 38, p. 1590, 1991.
[172] M. Shibuya, S. Mitsumoto, H. Nakano, S. Ishii, and H. Kojima, "Temperature dependence of annealing of gamma-ray radiation damage on SOS transistors," *IEEE Trans. Nucl. Sci.*, vol. NS-31, p. 1289, 1984.
[173] J.-L. Leray, "Activation energies of oxide charge recovery in SOS or SOI structures after an ionizing pulse," *IEEE Trans. Nucl. Sci.*, vol. NS-32, p. 3921, 1985.
[174] C.-H. Ang, C.-H. Ling, Z.-Y. Cheng, S.-J. Kim, and B.-J. Cho, "Bias and thermal annealings of radiation-induced leakage currents in thin-gate oxides," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 2758, 2000.
[175] T. Carriere, J. Beaucour, A. Gach, B. Johlander, and L. Adams, "Dose rate and annealing effects on total dose response of MOS and bipolar circuits," *IEEE Trans. Nucl. Sci.*, vol. 42, p. 1567, 1995.
[176] A. B. Jaksic, M. M. Pejovic, and G. S. Ristic, "Isothermal and isochronal annealing experiments on irradiated commercial power VDMOSFETS," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 659, 2000.
[177] G. S. Ristic, M. M. Pejovic, and A. B. Jaksic, "Modeling of kinetics of creation and passivation of interface traps in metal-oxide-semiconductor transistors during postirradiation annealing," *J. Appl. Phys.*, vol. 83, p. 2994, 1998.
[178] A. Kelleher, W. Lane, and L. Adams, "Investigation of on-chip high temperature annealing of PMOS dosimeters," *IEEE Trans. Nucl. Sci.*, vol. 43, p. 997, 1996.
[179] F. Saigne, L. Dusseau, J. Fesquet, J. Gasiot, R. Ecoffet, R. D. Schrimpf, and K. F. Galloway, "Prediction of the one-year thermal annealing of irradiated commercial devices based on experimental isochronal curves," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 2244, 2000.
[180] H. Scarpulla, R. Mozulay, C. Ausnit, E. W. Hogan, and R. H. Casey, "Rapid annealing response of the hardened 1802 bulk CMOS microprocessor," *IEEE Trans. Nucl. Sci.*, vol. NS-27, p. 1442, 1980.

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

[181] N. D. Wilkin and C. T. Self, "Temperature effects on failure and annealing behavior in dynamic random access memories," *IEEE Trans. Nucl. Sci.*, vol. NS-29, p. 1669, 1982.
[182] J. R. Schwank, P. S. Winokur, P. J. McWhorter, F. W. Sexton, P. V. Dressendorfer, and D. C. Turpin, "Physical mechanisms contributing to device 'Rebound'," *IEEE Trans. Nucl. Sci.*, vol. NS-31, p. 1434, 1984.
[183] C. M. Dozier, D. B. Brown, J. L. Throckmorton, and D. I. Ma, "Defect production in SiO_2 by X-ray and Co-60 radiations," *IEEE Trans. Nucl. Sci.*, vol. NS-32, p. 4363, 1985.
[184] A. J. Lelis and T. R. Oldham, "Time dependence of switching oxide traps," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 1835, 1994.
[185] D. M. Fleetwood, P. S. Winokur, R. A. Reber, T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt, and L. C. Riewe, "Effects of oxide traps, interface traps, and 'border traps' on metal-oxide-semiconductor devices," *J. Appl. Phys.*, vol. 73, p. 5058, 1993.
[186] D. M. Fleetwood and N. S. Saks, "Oxide, interface, and border traps in thermal, N_2O, and N_2O-nitrided oxides," *J. Appl. Phys.*, vol. 79, p. 1583, 1996.
[187] J. F. Conley, P. M. Lenahan, A. J. Lelis, and T. R. Oldham, "Electron spin resonance evidence for the structure of a switching oxide trap: Long term structural change at silicon dangling bond sites in SiO_2," *Appl. Phys. Lett.*, vol. 67, p. 2179, 1995.
[188] ——, "Electron spin resonance evidence that E' centers can behave as switching oxide traps," *IEEE Trans. Nucl. Sci.*, vol. 42, p. 1744, 1995.
[189] R. E. Stahlbush, "Slow and fast state formation caused by hydrogen," in *The Physics and Chemistry of SiO_2 and the Si–SiO_2 Interface (3)*, H. Z. Massoud, E. H. Poindexter, and C. R. Helms, Eds. Pennington, NJ: The Electrochemical Society, 1996, vol. 96-1, p. 525.
[190] E. H. Poindexter, "MOS interface states: Overview and physicochemical perspective," *Semiconduct. Sci. Technol.*, vol. 4, p. 961, 1989.
[191] T. P. Ma, "Interface trap transformation in radiation or hot-electron damaged MOS structures," *Semiconduct. Sci. Technol.*, vol. 4, p. 1061, 1989.
[192] F. B. McLean, "A framework for understanding radiation-induced interface states in SiO_2 MOS structures," *IEEE Trans. Nucl. Sci.*, vol. NS-27, p. 1651, 1980.
[193] T. R. Oldham, F. B. McLean, H. E. Boesch, and J. M. McGarrity, "An overview of radiation-induced interface traps in MOS structures," *Semiconduct. Sci. Technol.*, vol. 4, p. 986, 1989.
[194] D. B. Brown and N. S. Saks, "Time dependence of radiation-induced interface trap formation in metal-oxide-semiconductor devices as a function of oxide thickness and applied field," *J. Appl. Phys.*, vol. 70, p. 3734, 1991.
[195] N. S. Saks and R. W. Rendell, "The time-dependence of post-irradiation interface trap build-up in deuterium-annealed oxides," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 2220, 1992.
[196] M. L. Reed and J. D. Plummer, "Two reaction model of interface trap annealing," *IEEE Trans. Nucl. Sci.*, vol. NS-33, p. 1198, 1986.
[197] ——, "Chemistry of Si–SiO_2 interface trap annealing," *J. Appl. Phys.*, vol. 63, p. 5776, 1988.
[198] M. L. Reed, "Models of Si–SiO_2 interface reactions," *Semiconduct. Sci. Technol.*, vol. 4, p. 980, 1989.
[199] K. Vanheusden, R. A. B. Devine, J. R. Schwank, D. M. Fleetwood, R. G. Polcawich, W. L. Warren, S. P. Karna, and R. D. Pugh, "Irradiation response of mobile protons in buried SiO_2 films," *IEEE Trans. Nucl. Sci.*, vol. 44, p. 2087, 1997.
[200] R. E. Stahlbush, "The effects of radiation-induced defects on H^+ transport in SiO_2," *Microelectron. Eng.*, vol. 48, p. 215, 1999.
[201] G. Singh, K. F. Galloway, and T. J. Russell, "Temperature-Induced rebound in power MOSFETS," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1366, 1987.
[202] C.-T. Sah, J. Y.-C. Sun, and J. J.-T. Tzou, "Deactivation of the boron acceptor in silicon by hydrogen," *Appl. Phys. Lett.*, vol. 43, p. 204, 1983.
[203] J. I. Pankove, "Temperature dependence of boron neutralization in silicon by atomic hydrogen," *J. Appl. Phys.*, vol. 68, p. 6532, 1990.
[204] J. I. Pankove, D. E. Carlson, J. E. Berkeyheiser, and R. O. Wance, "Neutralization of shallow acceptor levels in silicon by atomic hydrogen," *Phys. Rev. Lett.*, vol. 51, p. 2224, 1983.
[205] M. R. Shaneyfelt, R. L. Pease, J. R. Schwank, M. C. Maher, G. L. Hash, D. M. Fleetwood, P. E. Dodd, C. A. Reber, S. C. Witczak, L. C. Riewe, H. P. Hjalmarson, J. C. Banks, B. L. Doyle, and J. A. Knapp, "Impact of passivation layers on enhanced low-dose-rate sensitivity and thermal-stress effects in linear bipolar IC's," *IEEE Trans. Nucl. Sci.*, vol. 49, 2002.
[206] M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, T. L. Meisenheimer, and P. S. Winokur, "Effects of burn-in on radiation hardness," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 2550, 1994.
[207] J. I. Pankove, R. O. Wance, and J. E. Berkeyheiser, "Neutralization of acceptors in silicon by atomic hydrogen," *Appl. Phys. Lett.*, vol. 45, p. 1100, 1984.
[208] S. C. Witczak, R. C. Lacoe, D. C. Mayer, D. M. Fleetwood, R. D. Schrimpf, and K. F. Galloway, "Space charge limited degradation of bipolar oxides at low electric fields," *IEEE Trans. Nucl. Sci.*, vol. 45, p. 2339, 1998.
[209] S. C. Witczak, R. C. Lacoe, M. R. Shaneyfelt, D. C. Mayer, J. R. Schwank, and P. S. Winokur, "Implications of radiation-induced dopant deactivation for NPN bipolar junction transistors," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 2281, 2000.
[210] V. V. Afanas'ev and A. Stesmans, "Proton nature of radiation-induced positive charge in SiO_2 layers on Si," *Europhys. Lett.*, vol. 53, p. 233, 2001.
[211] R. K. Reich, J. W. Schrankler, D.-H. Ju, M. S. Holt, and G. D. Kirchner, "Radiation-Dependent hot-carrier effects," *IEEE Electron. Device Lett.*, vol. EDL-7, p. 235, 1986.
[212] J. D. McBrayer, D. M. Fleetwood, R. A. Pastorek, and R. V. Jones, "Correlation of hot-carrier and radiation effects in MOS transistors," *IEEE Trans. Nucl. Sci.*, vol. NS-32, p. 3935, 1985.
[213] R. L. Woodruff and J. R. Adams, "Radiation effects in LDD MOS devices," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1629, 1987.
[214] G. P. Nelson and E. E. King, "Methods for radiation testing random access memories and LSI circuits," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2341, 1977.
[215] W. J. Poch and A. G. Holmes-Siedle, "The long-term effects of radiation on complementary MOS logic networks," *IEEE Trans. Nucl. Sci.*, vol. NS-17, p. 33, 1970.
[216] N. Kaul, B. L. Bhuva, V. Rangavajjhala, H. v. d. Molen, and S. E. Kerns, "Simulation of design dependent failure exposure levels for CMOS IC's," *IEEE Trans. Nucl. Sci.*, vol. 37, p. 2097, 1990.
[217] O. Quittard, F. Joffre, C. Brisset, C. Oudea, F. Saigne, L. Dusseau, J. Fesquet, and J. Gasiot, "Use of the radiation-induced charge neutralization mechanism to achieve annealing of 0.35 micron SRAM's," *IEEE Trans. Nucl. Sci.*, vol. 46, p. 1633, 1999.
[218] P. S. Winokur, F. W. Sexton, G. L. Hash, and D. C. Turpin, "Total-dose failure mechanisms of integrated circuits in laboratory and space environments," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1448, 1987.
[219] M. D. Lantz and K. F. Galloway, "Total dose effects on circuit speed measurements," *IEEE Trans. Nucl. Sci.*, vol. NS-30, p. 4264, 1983.
[220] B. R. Blaes, M. G. Buehler, and Y. S. Lin, "Propagation delay measurements from a timing sampler intended for use in space," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1470, 1987.
[221] C. P. Brothers and R. D. Pugh, "Simulating total-dose and dose-rate effects on digital microelectronics timing delays using VHDL," *IEEE Trans. Nucl. Sci.*, vol. 42, p. 1628, 1995.
[222] L. L. Sivo and P. R. Measel, "Radiation hardness of CMOS LSI circuits," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2219, 1977.
[223] D. M. Fleetwood, P. S. Winokur, and T. L. Meisenheimer, "Hardness assurance for low-dose space applications," *IEEE Trans. Nucl. Sci.*, vol. 38, p. 1552, 1991.
[224] F. W. Sexton, D. M. Fleetwood, C. C. Aldridge, G. Garrett, J. C. Pelletier, and J. I. Gaona, "Qualifying commerical IC's for space total-dose environments," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 1869, 1992.
[225] G. E. Davis, L. R. Hite, T. G. W. Blake, C.-E. Chen, H. W. Lam, and R. DeMoyer, "Transient radiation effects in SOI memories," *IEEE Trans. Nucl. Sci.*, vol. NS-32, p. 4432, 1985.
[226] G. J. Brucker, J. Wert, and P. Measel, "Transient imprint memory effect in MOS memories," *IEEE Trans. Nucl. Sci.*, vol. NS-33, p. 1484, 1986.
[227] D. M. Fleetwood and P. V. Dressendorfer, "A simple method to identify radiation and annealing biases that lead to worst-case CMOS static RAM postirradiation response," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1408, 1987.
[228] R. Brueckner, "Properties and structure of vitreous silica, II," *J. Non-Cryst. Solids*, vol. 5, p. 177, 1971.
[229] G. H. Sigel and B. D. Evans, "Effects of ionizing radiation on transmission of optical fibers," *Appl. Phys. Lett.*, vol. 24, p. 410, 1974.
[230] D. L. Griscom, "Point defects in amorphous SiO_2: What have we learned from 30 years of experimentation?," *Defects Glasses*, vol. 61, p. 213, 1986.
[231] E. J. Friebele, G. H. Sigel, and M. E. Gingerich, "Radiation response of fiber optic waveguides in the 0.4 to 1.7 micron region," *IEEE Trans. Nucl. Sci.*, vol. NS-25, p. 1261, 1978.
[232] E. J. Friebele, C. G. Askins, M. E. Gingerich, and K. J. Long, "Optical fiber waveguides in radiation environments, II," *Nuclear Instrum. Methods Phys. Res.*, vol. B1, p. 355, 1984.

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

[233] E. J. Friebele, E. W. Taylor, G. T. D. Beauregard, J. A. Wall, and C. E. Barnes, "Interlaboratory comparison of radiation-induced attenuation in optical fibers. Part I: Steady-state exposures," *J. Lightwave Technol.*, vol. 6, p. 165, 1988.

[234] G. J. Brucker, "Transient and steady-state radiation response of CMOS/SOS devices," *IEEE Trans. Nucl. Sci.*, vol. NS-21, p. 201, 1974.

[235] I. Yoshii, K. Hama, and K. Maeguchi, "Radiation effects on p^+ poly gate MOS structures with thin oxides," *IEEE Trans. Nucl. Sci.*, vol. 36, p. 2124, 1989.

[236] J. M. Benedetto, H. E. Boesch, T. R. Oldham, and G. A. Brown, "Measurement of low-energy X-ray dose enchancement in MOS devices with metal silicide gates," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1540, 1987.

[237] Y. Nishioka, E. F. d. Silva, and T.-P. Ma, "Radiation-Induced interface traps in Mo/SiO_2/Si capacitors," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1166, 1987.

[238] R. K. Smeltzer, "Refractory gate technology for radiation hardened circuits," *IEEE Trans. Nucl. Sci.*, vol. NS-27, p. 1745, 1980.

[239] R. Lin, Q. Lu, P. Ranade, T.-J. King, and C. Hu, "An adjustable work funtion technology using Mo gate for CMOS devices," *IEEE Electron. Devices Lett.*, vol. 23, p. 49, 2002.

[240] V. Zekeriya and T. P. Ma, "Dependence of radiation-induced interface traps on gate electrode material in metal/SiO_2/Si devices," *Appl. Phys. Lett.*, vol. 47, p. 54, 1985.

[241] S.-C. Lee, A. Raparla, Y. F. Li, G. Gasiot, R. D. Schrimpf, D. M. Fleetwood, K. F. Galloway, M. Featherby, and D. Johnson, "Total dose effects in composite nitride-oxide films," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 2297, 2000.

[242] W. Poch and A. G. Holmes-Siedle, "Permanent radiation effects in complementary-symmetry MOS integrated circuits," *IEEE Trans. Nucl. Sci.*, vol. NS-16, p. 227, 1969.

[243] J. Lindmayer and W. P. Noble, "Radiation resistant MOS devices," *IEEE Trans. Electron. Devices*, vol. ED-15, p. 637, 1968.

[244] N. S. Saks, J. M. Killiany, P. R. Reid, and W. D. Baker, "A radiation hard MNOS CCD for low temperature applications," *IEEE Trans. Nucl. Sci.*, vol. NS-26, p. 5074, 1979.

[245] M. H. White, D. A. Adams, and J. Bu, "On the go with SONOS," *IEEE Circuits and Devices*, vol. 16, p. 22, 2000.

[246] S. T. Liu, P. Fechner, S. Balster, G. Dougal, S. Sinha, H. Chen, G. Shaw, J. Yue, W. C. Jenkins, and H. L. Hughes, "A 5 nm nitrided gate oxide for 0.25 micron SOI CMOS technologies," *IEEE Trans. Nucl. Sci.*, vol. 46, p. 1824, 1999.

[247] R. E. Stahlbush, "Electron trapping in buried oxides during irradiation at 40 and 300 K," *IEEE Trans. Nucl. Sci.*, vol. 43, p. 2627, 1996.

[248] J. F. Conley, P. M. Lenahan, and P. Roitman, "Evidence for a deep electron trap and charge compensation in separation by implanted oxygen oxides," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 2114, 1992.

[249] R. Gale, F. J. Feigl, C. W. Magee, and D. R. Young, "Hydrogen migration under avalanche injection of electrons in Si metal-oxide-semiconductor capacitors," *J. Appl. Phys.*, vol. 54, p. 6938, 1983.

[250] H. Uchida and T. Ajioka, "Electron trap center generation due to hole trapping in SiO_2 under Fowler-Nordheim tunneling stress," *Appl. Phys. Lett.*, vol. 51, p. 433, 1987.

[251] R. J. Powell, "Hole photocurrents and electron tunnel injection induced by trapped holes in SiO_2 films," *J. Appl. Phys.*, vol. 46, p. 4557, 1975.

[252] S. Scharf, M. Schmidt, F. Wulf, and D. Braunig, "Comparison of the generation of interface states in MOS structures due to ^{60}Co and VUV irradiation accompanied with photoinjection of electrons," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 460, 1994.

[253] R. K. Lawrence and D. E. Ioannou, "Electron traps on high-temperature oxidized SIMOX buried oxides," *IEEE Trans. Electron. Devices Lett.*, vol. 17, p. 341, 1996.

[254] Z. Shanfield and M. M. Moriwaki, "Characteristics of hole traps in dry and pyrogenic gate oxides," *IEEE Trans. Nucl. Sci.*, vol. NS-31, p. 1242, 1984.

[255] D. M. Fleetwood, R. A. Reber, and P. S. Winokur, "Effect of bias on thermally stimulated current (TSC) in irradiated MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 38, p. 1066, 1991.

[256] R. A. Reber and D. M. Fleetwood, "Thermally stimulated current measurements of SiO_2 defect density and energy in irradiated metal-oxide-semiconductor capacitors," *Rev. Sci. Instrum.*, vol. 63, p. 5714, 1992.

[257] D. M. Fleetwood, S. L. Miller, R. A. Reber, P. J. McWhorter, P. S. Winokur, M. R. Shaneyfelt, and J. R. Schwank, "New insights into radiation-induced oxide-trap charge through thermally-stimulated-current measurement and analysis," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 2192, 1992.

[258] W. J. Dennehy, A. G. Holmes-Siedle, and K. H. Zaininger, "Process techniques and radiation effects in metal-insulator semiconductor structures," *IEEE Trans. Nucl. Sci.*, vol. NS-14, p. 276, 1967.

[259] A. Stesmans, V. V. Afanas'ev, and A. G. Revesz, "Suppression of thermal interface degradation in (111) Si/SiO_2 by noble gases," *Appl. Phys. Lett.*, vol. 74, p. 1466, 1999.

[260] Y. Wang, T. P. Ma, and R. C. Barker, "Orientation dependence of interface-trap transformation," *IEEE Trans. Nucl. Sci.*, vol. 36, p. 1784, 1989.

[261] R. E. Stahlbush, R. K. Lawrence, H. L. Hughes, and N. S. Saks, "Annealing of total dose damage: Redistribution of interface state density on $\langle 100 \rangle$, $\langle 110 \rangle$, and $\langle 111 \rangle$ orientation silicon," *IEEE Trans. Nucl. Sci.*, vol. 35, p. 1192, 1988.

[262] E. H. Poindexter, P. J. Caplan, B. E. Deal, and R. R. Razouk, "Interface states and electron spin resonance centers in thermally oxidized (111) and (100) silicon wafers," *J. Appl. Phys.*, vol. 52, p. 879, 1981.

[263] E. F. daSilva, Y. Nishioka, and T.-P. Ma, "Effects of trichloroethane during oxide growth on radiation-induced interface traps in metal/SiO_2/Si capacitors," *Appl. Phys. Lett.*, vol. 51, p. 1262, 1987.

[264] Y. Wang, Y. Nishioka, T. P. Ma, and R. C. Barker, "Radiation and hot-electron effects on SiO2/Si interfaces with oxides grown in O_2 containing small amounts of trichloroethane," *Appl. Phys. Lett.*, vol. 52, p. 573, 1988.

[265] B. J. Mrstik, P. J. McMarr, R. K. Lawrence, and H. L. Hughes, "The use of spectroscopic ellipsometry to predict the radiation response of SIMOX," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 2277, 1994.

[266] B. J. Mrstik, V. V. Afanas'ev, A. Stesmans, P. J. McMarr, and R. K. Lawrence, "Relationship between oxide density and charge trapping in SiO_2 films," *J. Appl. Phy.*, vol. 85, p. 6577, 1999.

[267] B. J. Mrstik and P. J. McMarr, "Evidence of a long-range density gradient in SiO_2 films on Si from H_2-permeability measurements," *Phys. Rev. B*, vol. 48, p. 17 972, 1993.

[268] D. L. Griscom, "Defects in amorphous insulators," *J. Non-Crystalline Solids*, vol. 31, p. 241, 1978.

[269] W. L. Warren, M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, P. S. Winokur, and R. A. B. Devine, "Microscopic nature of border traps in MOS oxides," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 1817, 1994.

[270] R. A. B. Devine, "Oxygen gettering and oxide degradation during annealing of Si/SiO_2/Si structures," *J. Appl. Phys.*, vol. 77, p. 175, 1995.

[271] Y. Nishioka, K. Ohyu, Y. Ohji, M. Kato, E. F. daSilva, and T.-P. Ma, "Radiation hardened micron and submicron MOSFET's containing fluorinated oxides," *IEEE Trans. Nucl. Sci.*, vol. 36, p. 2116, 1989.

[272] Y. Nishioka, T. Itoga, K. Ohyu, M. Kato, and T.-P. Ma, "Radiation effects on fluorinated field oxides and associated devices," *IEEE Trans. Nucl. Sci.*, vol. 37, p. 2026, 1990.

[273] J. R. Schwank, D. M. Fleetwood, P. S. Winokur, P. V. Dressendorfer, D. C. Turpin, and D. T. Sanders, "The role of hydrogen in radiation-induced defect formation in polysilicon gate MOS devices," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1152, 1987.

[274] J. Krauser, F. Wulf, M. A. Briere, J. Steiger, and D. Braunig, "Study of hydrogen incorporation in MOS-structures after various process steps using nuclear reaction analysis (NRA)," *Microelectron. Eng.*, vol. 22, p. 65, 1993.

[275] J. Krauser, F. Wulf, and D. Braunig, "Measurement and analysis of hydrogen depth profiles in MOS-structures by using the ^{15}N nuclear reaction method," *J. Non-Cryst. Solids*, vol. 187, p. 264, 1995.

[276] M. A. Briere and D. Braunig, "A quantitative investigation of hydrogen in the metal-oxide-silicon system using NRA," *IEEE Trans. Nucl. Sci.*, vol. 37, p. 1658, 1990.

[277] V. V. Afanas'ev, G. J. Adriaenssens, and A. Stesmans, "Positive charging of thermal SiO_2 layers: Hole trapping versus proton trapping," *Microelectron. Eng.*, vol. 59, p. 85, 2001.

[278] B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, "Characteristics of the surface-state charge (Q_{ss}) of thermally oxidized silicon," *J. Electrochem. Soc.*, vol. 114, p. 266, 1967.

[279] M. H. Woods and R. Williams, "Hole traps in silicon dioxide," *J. Appl. Phys.*, vol. 47, p. 1082, 1976.

[280] F. J. Grunthaner and J. Maserjian, "Experimental observations of the chemistry of the SiO_2/Si interface," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2108, 1977.

[281] F. J. Grunthaner, B. F. Lewis, N. Zamini, J. Maserjian, and A. Madhukar, "XPS studies of structure-induced radiation effects at the Si/SiO_2 interface," *IEEE Trans. Nucl. Sci.*, vol. NS-27, p. 1640, 1980.

[282] F. J. Grunthaner, P. J. Grunthaner, and J. Maserjian, "Radiation-induced defects in SiO_2 as determined with XPS," *IEEE Trans. Nucl. Sci.*, vol. NS-29, p. 1462, 1982.

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

[283] G. H. Sigel, E. J. Friebele, R. J. Ginther, and D. L. Griscom, "Effects of stoichiometry on the radiation response of SiO_2," *IEEE Trans. Nucl. Sci.*, vol. NS-21, p. 56, 1974.

[284] B. J. Mrstik, H. L. Hughes, P. J. McMarr, R. K. Lawrence, D. I. Ma, I. P. Isaacson, and R. A. Walker, "Hole and electron trapping in ion implanted thermal oxides and SIMOX," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 2189, 2000.

[285] B. J. Mrstik, H. L. Hughes, R. K. Lawrence, P. J. McMarr, and P. Gouker, "Comparison of charge trapping in undoped oxides made by low- and high-temperature deposition techniques," *IEEE Trans. Nucl. Sci.*, vol. 48, p. 2107, 2001.

[286] D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, "The electronic structure at the atomic scale of ultrathin gate oxides," *Nature*, vol. 399, p. 758, 1999.

[287] B. J. Mrstik, V. V. Afanas'ev, A. Stesmans, and P. J. McMarr, "Relationship between hole trapping and oxide density in thermally grown SiO_2," *Microelectron. Eng.*, vol. 48, p. 143, 1999.

[288] S. Banerjee, S. Chakraborty, and P. T. Lai, "Evidence of swelling of SiO_2 upon thermal annealing," *Appl. Phys. Lett.*, vol. 80, p. 3075, 2002.

[289] P. J. McMarr, B. J. Mrstik, R. K. Lawrence, and G. G. Jernigan, "The radiation response of capacitors fabricated on bonded silicon-on-insulator substrates," *IEEE Trans. Nucl. Sci.*, vol. 44, p. 2115, 1997.

[290] A. G. Revesz, B. J. Mrstik, H. L. Hughes, and D. McCarthy, "Structure of SiO_2 films on silicon as revealed by oxygen transport," *J. Electrochem. Soc.*, vol. 133, p. 586, 1986.

[291] A. G. Revesz, W. Anwand, G. Brauer, H. L. Hughes, and W. Skorupa, "Density gradient in SiO_2 films on silicon as revealed by positron annihilation spectroscopy," *Appl. Surface Sci.*, vol. 194, p. 101, 2002.

[292] E. P. Eernisse, "Compaction of ion-implanted fused silica," *J. Appl. Phys.*, vol. 45, p. 167, 1974.

[293] R. A. B. Devine, "Radiation-sensitivity enhancement and annealing variation in densified, amorphous SiO_2," *Phys. Rev. B*, vol. 35, p. 35, 1987.

[294] A. G. Holmes-Siedle and K. H. Zaininger, "The physics of failure of MIS devices under radiation," *IEEE Trans. Reliability*, vol. R-17, p. 34, 1968.

[295] S. T. Liu and W. C. Jenkins, "The effect of power supply voltage scaling on the total dose radiation response of fully-depleted SOI MOS transistors," *IEEE Trans. Nucl. Sci.*, vol. 42, p. 2122, 1995.

[296] D. M. Fleetwood, P. V. Dressendorfer, and D. C. Turpin, "A reevaluation of worst-case postirradiation response for hardened MOS transistors," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1178, 1987.

[297] C. M. Dozier and D. B. Brown, "Effect of photon energy on the response of MOS devices," *IEEE Trans. Nucl. Sci.*, vol. NS-28, p. 4137, 1981.

[298] J. J. Tzou, J. Y.-C. Sun, and C.-T. Sah, "Field dependence of two large hole capture cross sections in thermal oxide on silicon," *Appl. Phys. Lett.*, vol. 43, p. 861, 1983.

[299] R. J. Krantz, L. W. Aukerman, and T. C. Zietlow, "Applied field and total dose dependence of trapped charge buildup in MOS devices," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1196, 1987.

[300] P. S. Winokur, E. B. Errett, D. M. Fleetwood, P. V. Dressendorfer, and D. C. Turpin, "Optimizing and controlling the radiation hardness of a Si-gate CMOS process," *IEEE Trans. Nucl. Sci.*, vol. NS-32, p. 3954, 1985.

[301] H. E. Boesch and T. L. Taylor, "Charge and interface state generation in field oxides," *IEEE Trans. Nucl. Sci.*, vol. NS-31, p. 1273, 1984.

[302] H. E. Boesch and F. B. McLean, "Hole transport and trapping in field oxides," *IEEE Trans. Nucl. Sci.*, vol. NS-32, p. 3940, 1985.

[303] O. Flament, D. Herve', O. Musseau, P. Bonnel, M. Raffaeli, J. L. Leray, J. Margail, B. Giffard, and A. J. Auberton-Herve', "Field dependent charge trapping effects in SIMOX buried oxides at very high dose," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 2132, 1992.

[304] H. E. Boesch and G. A. Brown, "Charge buildup at high dose and low fields in SIMOX buried oxides," *IEEE Trans. Nucl. Sci.*, vol. 6, p. 1234, 1991.

[305] R. K. Lawrence, D. E. Ioannou, H. L. Hughes, P. J. McMarr, and B. J. Mrstik, "Charge trapping versus buried oxide thickness for SIMOX structures," *IEEE Trans. Nucl. Sci.*, vol. 42, p. 2114, 1995.

[306] K. Kasama, F. Toyokawa, M. Tsukiji, M. Sakamoto, and K. Kobayashi, "Mechanical stress dependence of radiation effects in MOS structures," *IEEE Trans. Nucl. Sci.*, vol. NS-33, p. 1210, 1986.

[307] K. Kasama, M. Tsukiji, and K. Kobayashi, "Correlation between mechanical stress and hydrogen-related effects on radiation-induced damage in MOS structures," *IEEE Trans. Nucl. Sci.*, vol. NS-34, p. 1202, 1987.

[308] V. S. Pershenkov and V. V. Chuikin, "The effect of junction fringing fields on radiation-induced leakage current in oxide isolation structures," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 2044, 1992.

[309] T. Ohno, K. Izumi, M. Shimaya, and N. Shiono, "Radiation-hardened n-channel MOSFET achieved by a combination of polysilicon sidewall and SIMOX technology," *Electron. Lett.*, vol. 22, p. 559, 1986.

[310] L. Manchanda, S. J. Hillenius, W. T. Lynch, H.-I. Cong, K. K. Ng, and J. R. L. Field, "A high-performance directly insertable self-aligned ultra-rad-hard and enhanced isolation field-oxide technology for gigahertz silicon NMOS/CMOS VLSI," *IEEE Trans. Electron. Devices*, vol. 36, p. 651, 1989.

[311] D. G. Mavis and D. R. Alexander, "Employing radiation hardness by design techniques with commercial integrated circuit processes," in *Proc. Digital Avionics Systems Conf. (16th DASC, AIAA/IEEE)*, vol. 1, 1997, pp. 2.1–15.

[312] A. G. F. Dingwall and R. E. Stricker, "C^2L: A new high-density bulk CMOS technology," *IEEE J. Solid-State Circuits*, vol. 12, p. 344, 1977.

[313] A. G. F. Dingwall, R. E. Stricker, and J. O. Sinniger, "A high speed bulk CMOS C^2L microprocessor," *IEEE J. Solid-State Circuits*, vol. SC-12, p. 457, 1977.

[314] E. E. King and R. L. Martin, "Effects of total dose ionizing radiation on the 1802 microprocessor," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2172, 1977.

[315] L. S. Napoli, R. K. Smeltzer, R. Donnelly, and J. Yeh, "A radiation hardened 256×4 bulk CMOS RAM," *RCA Rev.*, vol. 43, p. 458, 1982.

[316] R. C. Lacoe, J. V. Osborn, R. Koga, S. Brown, and D. C. Mayer, "Applicatioin of hardness-by-design methodology to radiation-tolerant ASIC technologies," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 2334, 2000.

[317] J. M. Benedetto, A. Bishop, M. Martin, and N. Haddad, "High total dose response of the UTMC gate array fabricated at Lockheed Martin Federal Systems," in *Proc. IEEE Radiation Effects Data Workshop*, 1998, IEEE Catalog #98TH8385, p. 86.

[318] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Florian, A. Giraldo, E. Hejine, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, and W. Snoeys, "Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: Practical design aspects," *IEEE Trans. Nucl. Sci.*, vol. 46, p. 1690, 1999.

[319] H. Hatano and K. Doi, "Radiation-tolerant high-performance CMOS VLSI circuit design," *IEEE Trans. Nucl. Sci.*, vol. NS-32, p. 4031, 1985.

[320] H. Hatano and S. Takatsuka, "Total dose radiation-hardened latch-up free CMOS structures for radiation-tolerant VLSI designs," *IEEE Trans. Nucl. Sci.*, vol. NS-33, p. 1505, 1986.

[321] F. M. Roche and L. Salager, "CMOS inverter design-hardened to the total dose effect," *IEEE Trans. Nucl. Sci.*, vol. 43, p. 3097, 1996.

[322] C. F. Gibbon, D. H. Habing, and R. S. Flores, "A radiation-hard silicon gate bulk CMOS cell family," *IEEE Trans. Nucl. Sci.*, vol. NS-27, p. 1712, 1980.

[323] L. J. Palkuti and R. Pryor, "Radiation-hard CMOS/SOS standard circuits," *IEEE Trans. Nucl. Sci.*, vol. NS-23, p. 1715, 1976.

[324] R. Marec, P. Mary, R. Gaillard, J. M. Palau, G. Bruguier, and J. Gasiot, "A study involving the design and fabrication process on the SRAM behavior during a dose-rate event," *IEEE Trans. Nucl. Sci.*, vol. 43, p. 851, 1996.

[325] W. S. Kim, T. M. Mnich, W. T. Corbett, R. K. Treece, A. E. Giddings, and J. L. Jorgensen, "Radiation-hard design principles utilized in CMOS 8085 microprocessor family," *IEEE Trans. Nucl. Sci.*, vol. NS-30, p. 4229, 1983.

[326] J. R. Murray, "Design considerations for a radiation hardened nonvolatile memory," *IEEE Trans. Nucl. Sci.*, vol. 40, p. 1610, 1993.

[327] W. R. Dawes, T. A. Fischer, C. C.-C. Huang, W. J. Meyer, C. S. Smith, R. A. Blanchard, and T. J. Fortier, "Transient hardened power FETS," *IEEE Trans. Nucl. Sci.*, vol. NS-33, p. 1425, 1986.

[328] J. C. Desko, M. N. Darwish, M. C. Dolly, C. A. Goodwin, W. R. Dawes, and J. L. Titus, "Radiation hardening of a high voltage IC technology (BCDMOS)," *IEEE Trans. Nucl. Sci.*, vol. 37, p. 2083, 1990.

[329] A. Simone, I. Debusschere, A. Alaerts, and C. Claeys, "Ionizing radiation hardening of a CCD technology," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 1964, 1992.

[330] E.-S. Eid, T. Y. Chan, E. R. Fossum, R. H. Tsai, R. Spagnuolo, J. Deily, J. W. B. Byers, and J. C. Peden, "Design and characterization of ionizing radiation-tolerant CMOS APS image sensors up to 30 Mrd (Si) total dose," *IEEE Trans. Nucl. Sci.*, vol. 48, p. 1796, 2001.

[331] J. Bogaerts, B. Dierickx, G. Meynants, and D. Uwaerts, "Total dose and displacement damage effects in a radiation-hardened CMOS APS," *IEEE Trans. Electron. Devices*, vol. 50, p. 84, 2003.

[332] V. V. Afanas'ev, J. M. M. d. Nijs, and P. Balk, "SiO_2 hole traps with small cross section," *Appl. Phys. Lett.*, vol. 66, p. 1738, 1995.

[333] D. J. DiMaria, Z. A. Weinburg, and J. M. Aitken, "Location of positive charges in SiO_2 films on Si generated by VUV photons, X-rays, and high-field stressing," *J. Appl. Phys.*, vol. 48, p. 898, 1977.

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

[334] W. L. Warren, D. M. Fleetwood, M. R. Shaneyfelt, J. R. Schwank, P. S. Winokur, R. A. B. Devine, and D. Mathiot, "Links between oxide, interface, and border traps in high-temperature annealed Si/SiO_2 systems," *Appl. Phys. Lett.*, vol. 64, p. 3452, 1994.

[335] B. J. Mrstik, P. J. McMarr, R. K. Lawrence, and H. L. Hughes, "A study of the radiation sensitivity of noncrystalline SiO_2 films using spectroscopic ellipsometry," *IEEE Trans. Nucl. Sci.*, vol. 45, p. 2450, 1998.

[336] K. Hofmann, D. R. Young, and G. W. Rubloff, "Hole trapping in SiO_2 films annealed in low-pressure oxygen atmosphere," *J. Appl. Phys.*, vol. 62, p. 925, 1987.

[337] M. Aslam, "Common origin for electron and hole traps in MOS devices," *IEEE Trans. Electron. Devices*, vol. ED-34, p. 2535, 1987.

[338] Z. A. Weinberg, D. R. Young, J. A. Calise, S. A. Cohen, J. C. DeLuca, and V. R. Deline, "Reduction of electron and hole trapping in SiO_2 by rapid thermal annealing," *Appl. Phys. Lett.*, vol. 45, p. 1204, 1984.

[339] V. V. Afanas'ev, A. Stesmans, A. G. Revesz, and H. L. Hughes, "Oxygen vacancies in SiO_2 layers on Si produced at high temperature," *J. Electrochem. Soc.*, vol. 145, p. 3157, 1998.

[340] R. J. Lambert, T. N. Bhar, and H. L. Hughes, "Effect of an augmented oxygen implant on electron trapping in buried oxides," *Appl. Phys. Lett.*, vol. 64, p. 3291, 1994.

[341] V. V. Afanas'ev and A. Stesmans, "Pressure dependence of Si/SiO_2 degradation suppression by helium," *J. Appl. Phys.*, vol. 87, p. 7338, 2000.

[342] D. J. DiMaria, J. M. Aitken, and D. R. Young, "Capture of electrons into Na^+-related trapping sites in the SiO_2 layer of MOS structures at 77°K," *J. Appl. Phys.*, vol. 47, p. 2740, 1976.

[343] A. Hartstein and D. R. Young, "Identification of electron traps in thermal silicon dioxide films," *Appl. Phys. Lett.*, vol. 38, p. 631, 1981.

[344] T. H. Ning, "Thermal reemission of trapped electrons in SiO_2," *J. Appl. Phys.*, vol. 49, p. 5997, 1978.

[345] M. Aslam, "Electron self-trapping in SiO_2," *J. Appl. Phys.*, vol. 62, p. 159, 1987.

[346] T. H. Ning, C. M. Osburn, and H. N. Yu, "Electron trapping at positively charged centers in SiO_2," *Appl. Phys. Lett.*, vol. 26, p. 248, 1975.

[347] D. R. Young, "Characterization of electron traps in SiO_2 as influenced by processing parameters," *J. Appl. Phys.*, vol. 52, p. 4090, 1981.

[348] S. K. Lai, D. R. Young, J. A. Calise, and F. J. Feigl, "Reduction of electron trapping in silicon dioxide by high-temperature nitrogen anneal," *J. Appl. Phys.*, vol. 52, p. 5691, 1981.

[349] P. Balk, M. Aslam, and D. R. Young, "High temperature annealing behavior of electron traps in thermal SiO_2," *Solid State Electron.*, vol. 27, p. 709, 1984.

[350] J. M. Aitken and D. R. Young, "Electron trapping by radiation-induced charge in MOS devices," *J. Appl. Phys.*, vol. 47, p. 1196, 1976.

[351] J. M. Aitken, D. R. Young, and K. Pan, "Electron trapping in electron-beam irradiated SiO_2," *J. Appl. Phys.*, vol. 49, p. 3386, 1978.

[352] A. Reisman, C. J. Merz, J. R. Maldonado, and W. W. Molzen, "Low energy X-ray and electron damage to IGFET gate insulators," *J. Electr. Chem. Soc.*, vol. 131, p. 1404, 1984.

[353] R. J. Reisman, M. Aitken, A. K. Ray, M. Berkenblit, C. J. Merz, and R. P. Havreluk, "On the removal of insulator process induced radiation damage from insulated gate field effect transistors at elevated pressure," *J. Electrochem. Soc.*, vol. 128, p. 1616, 1981.

[354] P. K. Bhattacharya, A. Reisman, and M. C. Chen, "A controlled radiation source and electron/X-ray flux ratios in an electron beam metal evaporator," *J. Electron. Materials*, vol. 17, p. 273, 1988.

[355] M. Walters and A. Reisman, "The effects of various gate oxidation conditions on intrinsic and radiation-induced extrinsic charged defects and neutral electron traps," *J. Electrochem. Soc.*, vol. 137, p. 3596, 1990.

[356] C. T. Sune, A. Reisman, and C. K. Williams, "Defect generation in silicon-implanted gate insulators of insulated gate field-effect transistors," *J. Appl. Phys.*, vol. 66, p. 5801, 1989.

[357] ——, "Oxygen ion defect generation in insulated-gate field-effect transistors and X-radiation susceptibility of ion-damaged gate insulators," *J. Electrochem. Soc.*, vol. 137, p. 3574, 1990.

[358] S. Alexandrova and D. R. Young, "Microscopic location of electron traps induced by arsenic implantations in silicon dioxide," *J. Appl. Phys.*, vol. 54, p. 174, 1983.

[359] A. Kalnitsky, J. P. Ellul, E. H. Poindexter, P. J. Caplan, R. A. Lux, and A. R. Boothroyd, "Rechargeable E' centers in silicon-implanted SiO_2 films," *J. Appl. Phys.*, vol. 67, p. 7359, 1990.

[360] T. N. Bhar, R. J. Lambert, and H. L. Hughes, "Electron trapping in Si implanted SIMOX," *Electron. Lett.*, vol. 34, p. 1026, 1998.

[361] A. Mallik, J. Vasi, and A. N. Chandorkar, "Electron trapping during irradiation in reoxidized nitrided oxide," *IEEE Trans. Nucl. Sci.*, vol. 40, p. 1380, 1993.

[362] I. Rahat and J. Shappir, "Electron trapping in oxynitride layers in metal-oxide-semiconductor structures," *J. Appl. Phys.*, vol. 76, p. 2279, 1994.

[363] H. E. Boesch, T. L. Taylor, L. R. Hite, and W. E. Bailey, "Time-Dependent hole and electron trapping effects in SIMOX buried oxides," *IEEE Trans. Nucl. Sci.*, vol. 37, p. 1982, 1990.

[364] T. Ouisse, S. Cristoloveanu, and G. Borel, "Electron trapping in irradiated SIMOX buried oxides," *IEEE Electron. Devices Lett.*, vol. 12, p. 312, 1991.

[365] J. F. Conley and P. M. Lenahan, "A review of electron spin resonance spectroscopy of defects in thin film SiO_2 on Si," in *Proc. Electrochemical Soc. Third Int. Symp. Physics Chemistry of SiO_2 and the Si–SiO_2 Interface -3*, vol. 96-1, 1996, p. 214.

[366] O. Gruber, P. Paillet, O. Musseau, C. Marcandella, B. Aspar, and A. J. Auberton-Herve', "Physical characterization of electron trapping in UNIBOND® oxides," *IEEE Trans. Nucl. Sci.*, vol. 45, p. 1402, 1998.

[367] R. E. Stahlbush, G. J. Campisi, J. B. McKitterick, W. P. Maszara, P. Roitman, and G. A. Brown, "Electron and hole trapping in irradiated SIMOX, ZMR and BESOI buried oxides," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 2086, 1992.

[368] P. Paillet, D. Herve', J. L. Leray, and R. A. B. Devine, "Evidence of negative charge trapping in high temperature annealed thermal oxide," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 473, 1994.

[369] A. Meulenberg, "Radiation-hardened deposited oxides," *COMSAT Tech. Rev.*, vol. 18, p. 269, 1988.

[370] O. Flament, C. Chabrerie, V. Ferlet-Cavrois, J. L. Leray, F. Faccio, and P. Jarron, "A methodology to study lateral parasitic transistors in CMOS technologies," *IEEE Trans. Nucl. Sci.*, vol. 45, p. 1385, 1998.

[371] K. Watanabe, M. Kato, M. Nagata, and T. Okabe, "Radiation effects in SiO_2/Si structures," *Electron. Commun. Japan, Part 2*, vol. 71, p. 83, 1988.

[372] J. W. Lutze, A. H. Perera, and J. P. Krusius, "Field oxide thinning in poly buffer LOCOS isolation with active area spacings to 0.1 micron," *J. Electron. Chem. Soc.*, vol. 137, p. 1867, 1990.

[373] K. Neumeier and H. P. Bruemmer, "Radiation hard LOCOS field oxide," *IEEE Trans. Nucl. Sci.*, vol. 41, p. 572, 1994.

[374] F. T. Brady, J. D. Maimon, and M. J. Hurt, "A scaleable, radiation hardened shallow trench isolation," *IEEE Trans. Nucl. Sci.*, vol. 46, p. 1836, 1999.

[375] P. F. Schmidt, M. J. Rand, J. P. Mitchell, and J. D. Ashner, "Radiation-insensitive silicon oxynitride films for use in silicon devices (Part I)," *IEEE Trans. Nucl. Sci.*, vol. NS-16, p. 211, 1969.

[376] P. F. Schmidt and J. D. Ashner, "Radiation-Insensitive silicon oxynitride films for use in silicon devices—Part II," *IEEE Trans. Nucl. Sci.*, vol. NS-17, p. 11, 1970.

[377] H. A. R. Wegener, M. B. Doig, P. Marraffino, and B. Robinson, "Radiation resistant MNOS memories," *IEEE Trans. Nucl. Sci.*, vol. NS-19, p. 291, 1972.

[378] G. J. Dunn and P. W. Wyatt, "Reoxidized nitrided oxide for radiation-hardened MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 36, p. 2161, 1989.

[379] J. A. Dinitz, J. Godoy, P. J. Tatsch, and J. W. Swart, "Radiation hardening of oxynitrides formed by low energy nitrogen implantation into silicon prior to oxidation," *Electrochem. Soc. Meeting Abstracts*, vol. 2001-1, p. 263, 2001.

[380] R. A. Kjar, A. N. Lee, R. K. Pancholy, and J. L. Peel, "Self aligned radiation hard CMOS/SOS," *IEEE Trans. Nucl. Sci.*, vol. NS-23, p. 1610, 1976.

[381] S. N. Lee, R. A. Kjar, J. L. Peel, and G. Kinoshita, "Radiation-hardened silicon-gate CMOS/SOS," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2205, 1977.

[382] F. J. Kub, C. T. Yao, and J. R. Waterman, "Radiation hardened SOS MOSFET technology for infrared focal plane readouts," *IEEE Trans. Nucl. Sci.*, vol. 37, p. 2020, 1990.

[383] C. P. Chang, "Radiation hardened P-surface channel CCD's," *IEEE Trans. Nucl. Sci.*, vol. NS-23, p. 1639, 1976.

[384] ——, "Radiation effects in N-buried channel CCD's fabricated with a hardened process," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2190, 1977.

[385] J. M. Killiany, "Low-temperature radiation damage effects in a room-temperature radiation-hard surface channel CCD," *IEEE Trans. Nucl. Sci.*, vol. NS-24, p. 2194, 1977.

[386] C. P. Chang, "Radiation hardened N-buried channel CCD's using back-side phosphorus gettering," *IEEE Trans. Nucl. Sci.*, vol. NS-25, p. 1454, 1978.

[387] F. G. Broell and W. J. Barnard, "A radiation-hardened CMOS 8-Bit analog-to-Digital converter," *IEEE Trans. Nucl. Sci.*, vol. NS-30, p. 4246, 1983.

[388] G. B. Roper and R. Lowis, "Development of a radiation hard N-channel power MOSFET," *IEEE Trans. Nucl. Sci.*, vol. NS-30, p. 4110, 1983.

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.

[389] C. Picard, C. Brisset, O. Quittard, A. Hoffmann, F. Joffre, and J.-P. Charles, "Radiation hardening of power MOSFET's using electrical stress," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 641, 2000.
[390] P. M. Lenahan, J. F. Conley, and B. D. Wallace, "A model of hole trapping in SiO_2 films on silicon," *J. Appl. Phys.*, vol. 81, p. 6822, 1997.
[391] P. M. Lenahan, J. J. Mele, J. F. Conley, R. K. Lowry, and D. Woodbury, "Predicting radiation response from process parameters: Verification of a physically based predictive model," *IEEE Trans. Nucl. Sci.*, vol. 46, p. 1534, 1999.
[392] P. M. Lenahan and J. F. Conley, "What can electron paramagnetic resonance tell us about the Si/SiO_2 system?," *J. Vac. Sci. Technol. B*, vol. 16, p. 2134, 1998.
[393] S. P. Karna, H. A. Kurtz, W. M. Shedd, R. D. Pugh, and B. K. Singaraju, "New fundamental defects in a-SiO_2," *IEEE Trans. Nucl. Sci.*, vol. 46, p. 1544, 1999.
[394] D. L. Griscom, "Characterization of three E'-center variants in X- and gamma-irradiated high purity alpha-SiO_2," *Nucl. Instrum. Methods*, vol. B1, p. 481, 1984.
[395] A. G. Revesz, "Defect structure and irradiation behavior of noncrystalline SiO_2," *IEEE Trans. Nucl. Sci.*, vol. NS-18, p. 113, 1971.
[396] ——, "The defect structure of vitreous SiO_2 films on silicon II. Channel and network defects in vitreous SiO_2," *Phys. Stat. Sol.*, vol. A57, p. 235, 1980.
[397] E. H. Poindexter, "Physical chemistry of hydrogenous species in the Si–SiO_2 system," *Z. Naturforsch*, vol. 50a, p. 653, 1995.
[398] M. E. Zvanut, R. E. Stahlbush, W. E. Carlos, H. L. Hughes, R. K. Lawrence, R. Hevey, and G. A. Brown, "SIMOX with epitaxial silicon: Point defects and positive charge," *IEEE Trans. Nucl. Sci.*, vol. 38, p. 1253, 1991.
[399] D. Herve', J. L. Leray, and R. A. B. Devine, "Comparative study of radiation-induced electrical and spin active defects in buried SiO_2 layers," *J. Appl. Phys.*, vol. 72, p. 3634, 1992.
[400] R. K. Lawrence, B. J. Mrstik, H. L. Hughes, and P. J. McMarr, "Dependence of radiation induced buried oxide charge on silicon-on-insulator fabrication technology," *IEEE Trans. Nucl. Sci.*, vol. 43, p. 2639, 1996.
[401] B. J. Nicklaw, M. P. Pagey, S. T. Pantelides, D. M. Fleetwood, R. D. Schrimpf, K. F. Galloway, J. E. Wittig, B. M. Howard, E. Taw, W. H. McNeil, and J. F. Conley, "Defects and nanocrystals generated by Si implantation into a-SiO_2," *IEEE Trans. Nucl. Sci.*, vol. 47, p. 2269, 2000.
[402] F. W. Sexton, R. E. Anderson, W. T. Corbett, A. E. Giddings, J. L. Jorgensen, W. S. Kim, T. M. Mnich, T. V. Nordstrom, A. Ochoa, M. A. Sobolewski, R. K. Treece, and T. F. Wrobel, "Radiation testing of the CMOS 8085 microprocessor family," *IEEE Trans. Nucl. Sci.*, vol. NS-30, p. 4235, 1983.
[403] J. R. Schwank, M. R. Shaneyfelt, B. L. Draper, and P. E. Doss, "BUSFET—A radiation-hardened SOI transistor," *IEEE Trans. Nucl. Sci.*, vol. 46, p. 1809, 1999.
[404] J. M. Benedetto, "Economy-class ion-defying ICs in orbit," *IEEE Spectrum*, vol. 35, p. 36, 1998.
[405] A. J. Lelis and T. R. Oldham, "X-Ray lithography effects on MOS oxides," *IEEE Trans. Nucl. Sci.*, vol. 39, p. 2204, Dec. 1992.
[406] S. N. Rashkeev, D. M. Fleetwood, R. D. Schrimpf, and S.T. Pantelides, "Proton-induced defect generation at the Si-SiO_2 interface," *IEEE Trans. Nucl. Sci.*, vol. 48, p. 2086, 2001.
[407] A. Stesmans and V. V. Afanas'ev, "Invasive nature of corona charging on thermal Si/SiO_2 structures with nanometer-thick oxides revealed by electron spin resonance," *Appl. Phys. Lett.*, vol. 82, p. 2835, 2003.

Authorized licensed use limited to: INESC. Downloaded on December 10, 2009 at 12:04 from IEEE Xplore. Restrictions apply.